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THESIS

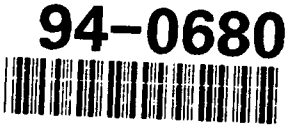
VLSI IMPLEMENTATION OF STRAY INSENSITIVE
SWITCHED CAPACITOR
COMPOSITE OPERATIONAL AMPLIFIERS

by

Gregory A. Silvernagel

December 1993

Thesis Advisor: Sherif Michael



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In this research, analog active circuits are implemented in VLSI technology by combining the properties of switched capacitors and composite amplifiers. This combined design improves upon the single operational amplifier's finite dc gain, limited bandwidth, lower slew rate, as well as enhancing the overall network passive and active sensitivities. The switched capacitor is implemented using both the toggle switched capacitor and the modified open floating resistor techniques. The composite operational amplifier is implemented using the C2OA-1 and C2OA-2 designs from the CNOA-*i* possibilites. These four designs are produced on a single microchip that includes the two phase non-overlapping clock circuit and the switches. The microchip is tested in a finite gain circuit and the results are used to evaluate the performance of the design. Short comings in the circuit performance are identified and the analysis is used to improve network simulations as well as provide guidance for design improvements. The design improvements are incorporated in a second generation microchip that is fabricated in a low noise analog process.

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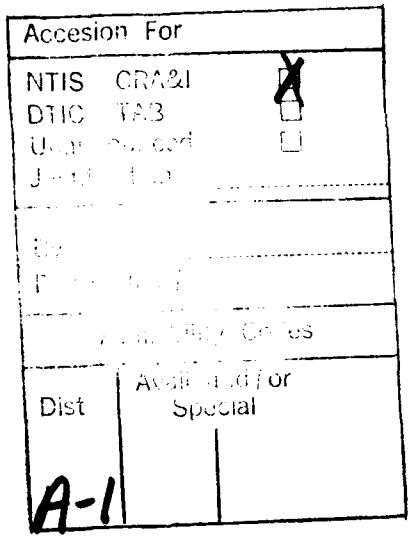
ABSTRACT

In this research, analog active circuits are implemented in VLSI technology by combining the properties of switched capacitors and composite amplifiers. This combined design improves upon the single operational amplifier's finite dc gain, limited bandwidth, lower slew rate, as well as enhancing the overall network passive and active sensitivities. The switched capacitor is implemented using both the toggle switched capacitor and the modified open floating resistor techniques. The composite operational amplifier is implemented using the C2OA-1 and C2OA-2 designs from the CNOA-*i* possibilites. These four designs are produced on a single microchip that includes the two phase non-overlapping clock circuit and the switches. The microchip is tested in a finite gain circuit and the results are used to evaluate the performance of the design. Short comings in the circuit performance are identified and the analysis is used to improve network simulations as well as provide guidance for design improvements. The design improvements are incorporated in a second generation microchip that is fabricated in a low noise analog process.



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I. INTRODUCTION

A. OVERVIEW

The operational amplifier (OA) is one of the most important analog integrated circuits in use today. This widespread use makes the OA a much needed part of Very Large Scale Integrated (VLSI) circuit designs. One of the difficulties arising from implementing an OA in a VLSI fabrication process is the large amount of area and the relative inaccuracies of producing resistors in the Complementary Metal Oxide Silicon (CMOS) process. This problem can be overcome by eliminating the resistors in the circuit and replacing them with switched capacitors. This will result in a size reduction and increased accuracy without resorting to expensive process techniques such as laser trimming. No additional or unique steps have to be added to the fabrication process to realize the benefits of this type of implementation.

Some limiting factors in the non-ideal performance of the OA can be eliminated or at least greatly improved by the use of composite operational amplifiers (CNOAs). Combining the CNOAs in a parasitic free switched capacitor network allows for circuit implementation on a single VLSI chip, as well as, provides considerable performance improvement and bandwidth extension over the single OA. This combination has direct applications in A/D and D/A conversion, digital communications, filtering, signal processing, speech processing, modulator-demodulator circuitry, HDTV, and neural network implementation to name a few.

This thesis proposes to build on previosly demonstrated stray insensitive switched capacitor composite operational amplifiers implemented with discrete small scale integrated and large scale integrated circuit components, with the purpose of implementing the circuits using a VLSI process. This will result in 22 discrete elements being implemented on a single microchip with the associated reduction in size, power consumption, etc.

B. EXISTING PROBLEMS AND SOLUTIONS

The amount of noise injected into the analog signal path from the digital portion of the circuit can cause unacceptable circuit performance degradation. This problem can be addressed by applying proper design techniques, layout topologies and using a fabrication process optimized for analog VLSI circuit implementation. Latchup is always a problem that must be addressed in CMOS processes. Fortunately, there are relatively simple design considerations which can prevent the failure of a circuit due to this problem which is inherent to CMOS implementations.

C. THESIS ORGANIZATION

The goal of this thesis was to demonstrate through design, simulation, fabrication and laboratory testing, the feasibility of implementing stray insensitive switched capacitor composite operational amplifiers on a single CMOS microchip. The stray insensitive switched capacitor composite operational amplifiers are briefly discussed in the second chapter. The third chapter discusses the CMOS process. The design and selection of the operational amplifiers is presented in the fourth chapter. The fifth chapter describes the

process of implementing the switches and the switched capacitors. The development of the clocking circuit is covered in chapter six and the design and implementation of the complete microchip is discussed in chapter seven. Chapter eight covers the problems encountered with the first microchip and it discusses the process used to fabricate the second design. The conclusions developed from this thesis are presented in chapter nine, as well as, recommendations for future research.

II. DISCRETE COMPONENT IMPLEMENTATION

A. WHY THE COMPOSITE OPERATIONAL AMPLIFIER

The operational amplifier (OA) is a widely used component in a variety of applications. The ideal OA has infinite input impedance, zero output impedance and infinite differential voltage gain. The practical OA, on the other hand, has several limitations such as finite dc gain, limited bandwidth, slow slew rate, finite input impedance and less than ideal output impedance. These limitations must be considered in any applications that use the operational amplifier. In many cases these characteristics are the limiting factor that prevent improvement in the performance of the circuit. Therefore, the need for an improved OA exists and the composite operational amplifier is a solution that provides many improvements over the single OA.

Composite Operational Amplifiers (CNOAs) were developed by S. N. Michael and W. B. Mikhael in 1981, their research and its applications have been published in References 1 - 7. The development of the CNOAs provided for a method to extend the operational frequency range (bandwidth) of linear active networks. The techniques used in the design of the CNOAs resulted in 136 possible circuits. After establishing performance criteria, the 136 designs were tested and four designs were selected that demonstrated superior performance according to the stringent performance criteria. Using the CNOA designation and replacing the N with the number of OAs employed, the four designs were labeled C2OA-1 through C2OA-4. Figure 2.1 illustrates the circuit diagrams

of the four composite operational amplifiers. These composite devices have three terminals which resemble the input and output terminals of a single OA.

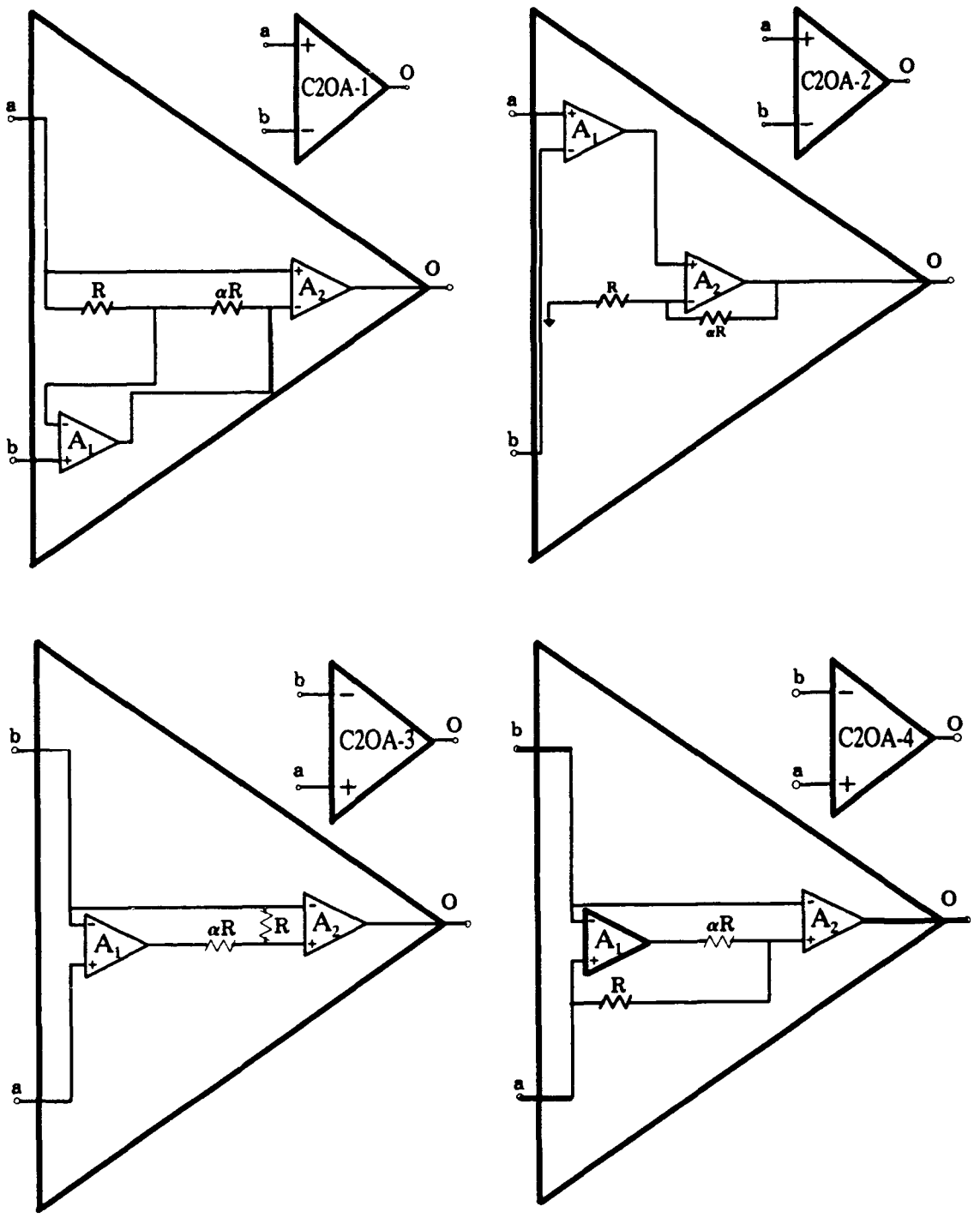


Figure 2.1 The Four CNOAs: C2OA-1, C2OA-2, C2OA-3, and C2OA-4

B. WHY SWITCHED CAPACITORS WITH THE CNOA

The primary reason for using switched capacitors to replace the resistors in the circuit comes from the desire to improve the VLSI implementation of the CNOA. Since resistors and capacitors are made at different steps in the fabrication process, their errors do not track one another. In addition, the temperature and voltage coefficients of resistors and capacitors are not correlated. Therefore, the time constants will vary with temperature and signal level. A solution to this problem is to replace the resistors in the circuit with switched capacitors.

The formula in Equation 2.1 is the governing principle by which the resistors in the circuit can be replaced by switched capacitors. This formula represents an approximation

$$R=\frac{1}{f_c C_R} \tag{2.1}$$

of the resistance that the capacitor is replacing. The f_c is the frequency of the clock used to switch the capacitor and C_R is the value of the capacitor that replaces the resistor in the circuit.

It has been shown in detail, in Reference 8, that, with proper clock frequency and phase a network of switched capacitors can emulate the operation and performance of a resistor in a circuit. The equivalent circuit replacement for the resistor results in smaller layout area and greatly reduced inaccuracies caused by process variations [Ref. 8:pp. 24 - 29].

Another important benefit to using switched capacitors is the ability to tune the operation of the circuit. The performance of the CNOA is dependent on α which is the ratio of the capacitors in the circuit. If this ratio was implemented using resistors in the CMOS process, the accuracy of α is typically no better than 10%, unless expensive laser trimming is used. But, if capacitors are used, the CMOS process can produce very accurate ratios between capacitors. This important ability is further explained in Chapter V.

C. STRAY INSENSITIVE SWITCHED CAPACITOR NETWORKS

One difficulty that must be addressed when using switched capacitors in circuit design is the internal stray (parasitic) capacitances. These parasitic capacitances are unpredictable and can significantly affect the performance of any switched capacitor network. Although the parasitic capacitances cannot be eliminated, their effect on the performance of the circuit can be nullified by choosing an appropriate switched capacitor topology.

There are few circuit topologies that can be used to nullify the effects of the lasting parasitic capacitances. Two topologies, investigated in Reference 8, that can prevent stray capacitance from adversely affecting a circuit are the toggle switched capacitor (TSC) and the modified open-circuit floating resistor (mOFR) techniques. Using the TSC and mOFR topologies, the composite operational amplifier designs C2OA-1 and C2OA-2 were chosen for a discrete implementation to determine the feasibility of the switched capacitor applications.

D. EXPERIMENTAL IMPLEMENTATION AND RESULTS

The four networks chosen to test the switched capacitor application were the C2OA-1 using the TSC topology, the C2OA-1 using the mOFR topology, the C2OA-2 using the TSC topology and the C2OA-2 using the mOFR topology. These networks were constructed with discrete components on a bread board and then tested to experimentally determine if the physical circuit performed as predicted by the theoretical calculations. The results of this testing clearly showed the physical circuit was in close agreement with the predicted performance parameters. A complete listing of the results of this testing can be found in Reference 8.

The following Figures 2.2 through 2.5 are functionally correct network diagrams of the four circuits that were tested. The Φ_e indicates the even phase of a two phase non-overlapping clock signal and Φ_o indicates the odd phase of the two phase non-overlapping clock signal. The C_R and the αC_R are the capacitors being used to replace resistors in the C2OA-1 and C2OA-2 composite amplifier designs. The α indicates that there is a ratio between the two capacitors. The **a** indicates the non-inverting input to the CNOA and the **b** indicates the inverting input to the CNOA. The **o** is the output terminal of the CNOA. The A_1 and A_2 labels are on symbols that represent standard single operational amplifiers.

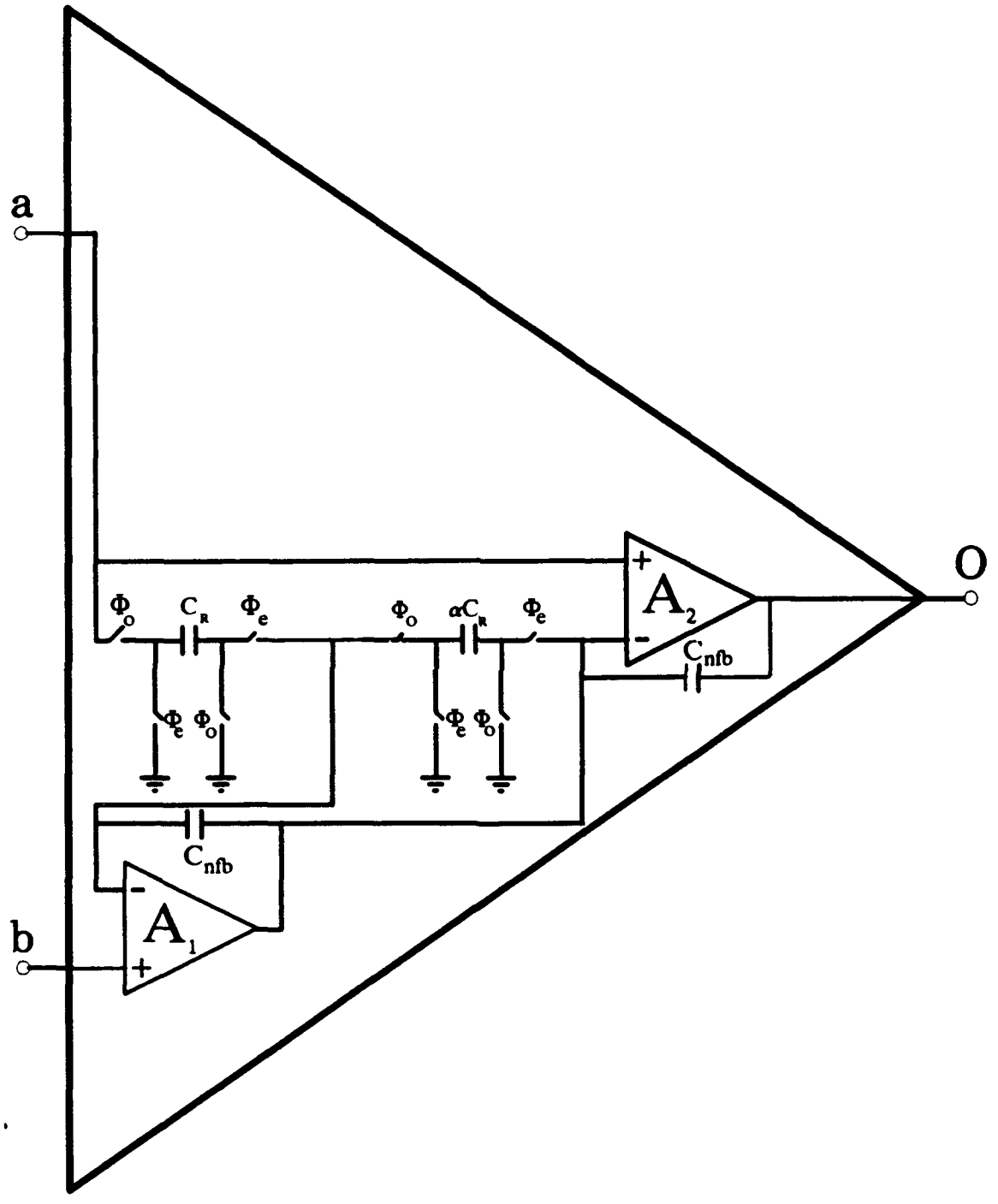


Figure 2.2 Stray Insensitive TSC C2OA-1

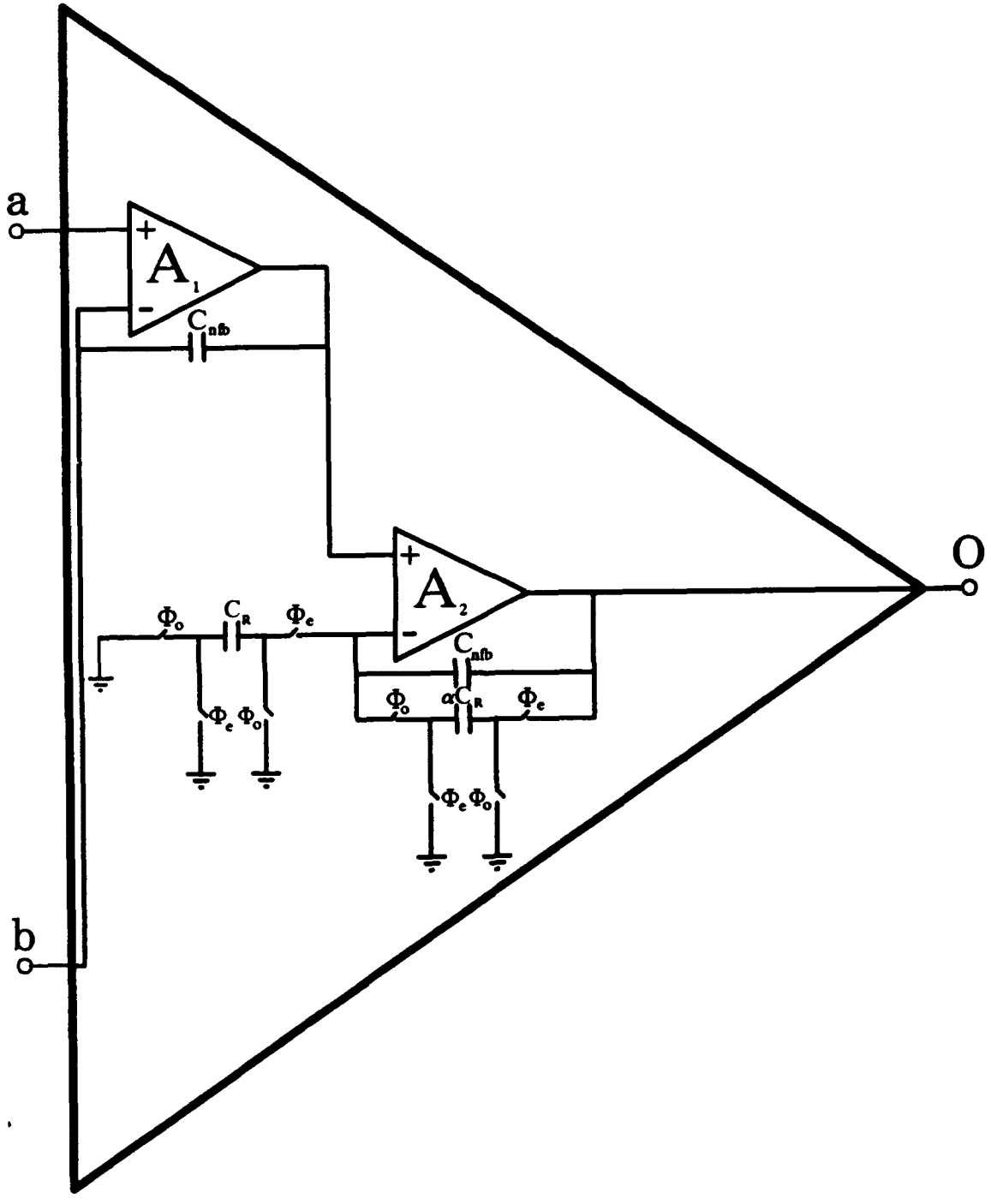


Figure 2.3 Stray Insensitive TSC C2OA-2

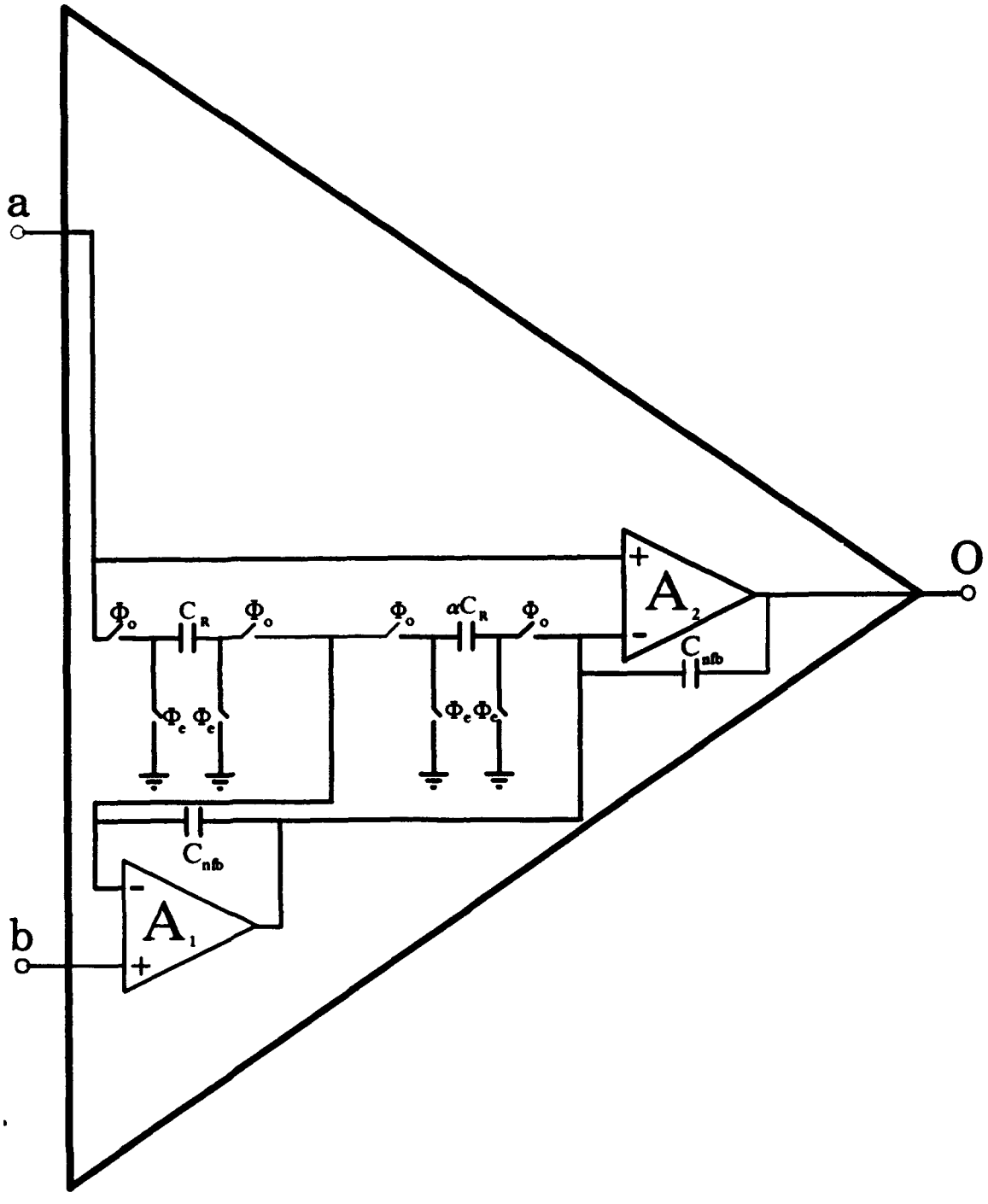


Figure 2.4 Stray Insensitive MOFR C2OA-1

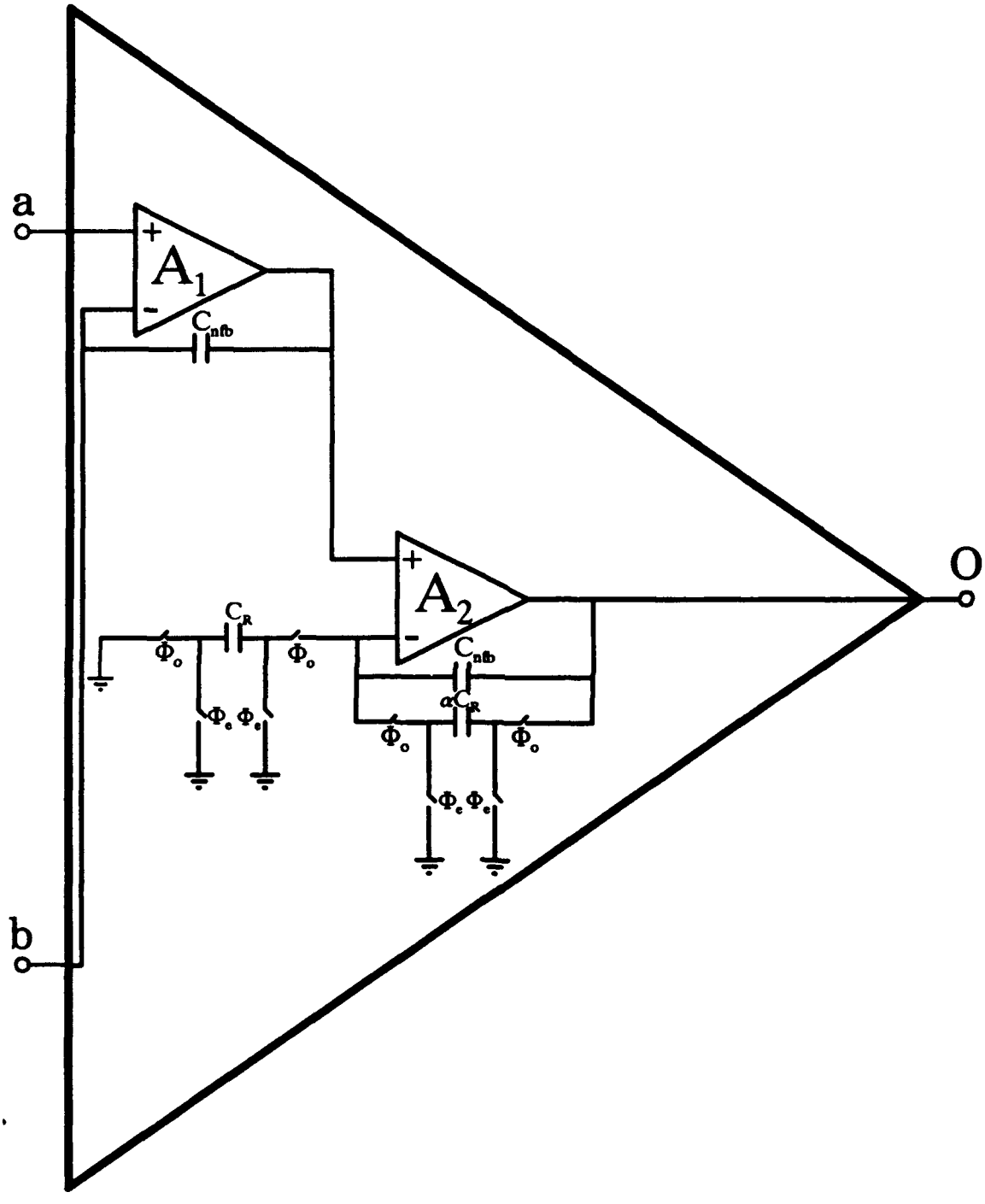


Figure 2.5 Stray Insensitive MOFR C2OA-2

III. THE CMOS PROCESS

A. SILICON SEMICONDUCTOR TECHNOLOGY

Silicon is the primary element used in the complementary metal oxide silicon (CMOS) process. Silicon in its pure form is a semiconductor, meaning that it's current carrying properties lie between that of a conductor and an insulator. By introducing certain types of impurities into the silicon crystal the conductivity of the silicon can be increased by several orders of magnitude. Depending on the type of impurity or dopant used the resulting material will become either n-type or p-type substrate. If the impurity provides excess free electrons, then it is called a donor element and it produces n-type material. If the impurity provides excess holes, then it is called an acceptor element and it produces p-type material.

The wafer is the initial product that is produced by semiconductor manufacturers. It is produced by adding the appropriate type and quantity of dopant to a container of molten silicon. A single seed crystal with the correct crystalline structure is lowered into the polycrystalline silicon melt and from this a long cylindrical crystal called an ingot is grown. This ingot is then sliced to produce the single wafers. The wafer that has been produced will provide either a p-type or n-type substrate on which the transistors will be produced.

B. PRODUCING NMOS AND PMOS TRANSISTORS

To produce an n-type metal oxide silicon (NMOS) transistor, the wafer must provide a p-type substrate. The substrate material will form the channel of the NMOS transistor. Figure 3.1 illustrates the different components of the NMOS transistor including the different layers and their arrangement.

To produce a p-type metal oxide silicon (PMOS) transistor, the wafer must provide an n-type substrate. As with the NMOS transistor, the substrate will form the channel of the PMOS transistor. Figure 3.2 illustrates the different components of the PMOS transistor including the different layers and their arrangement.

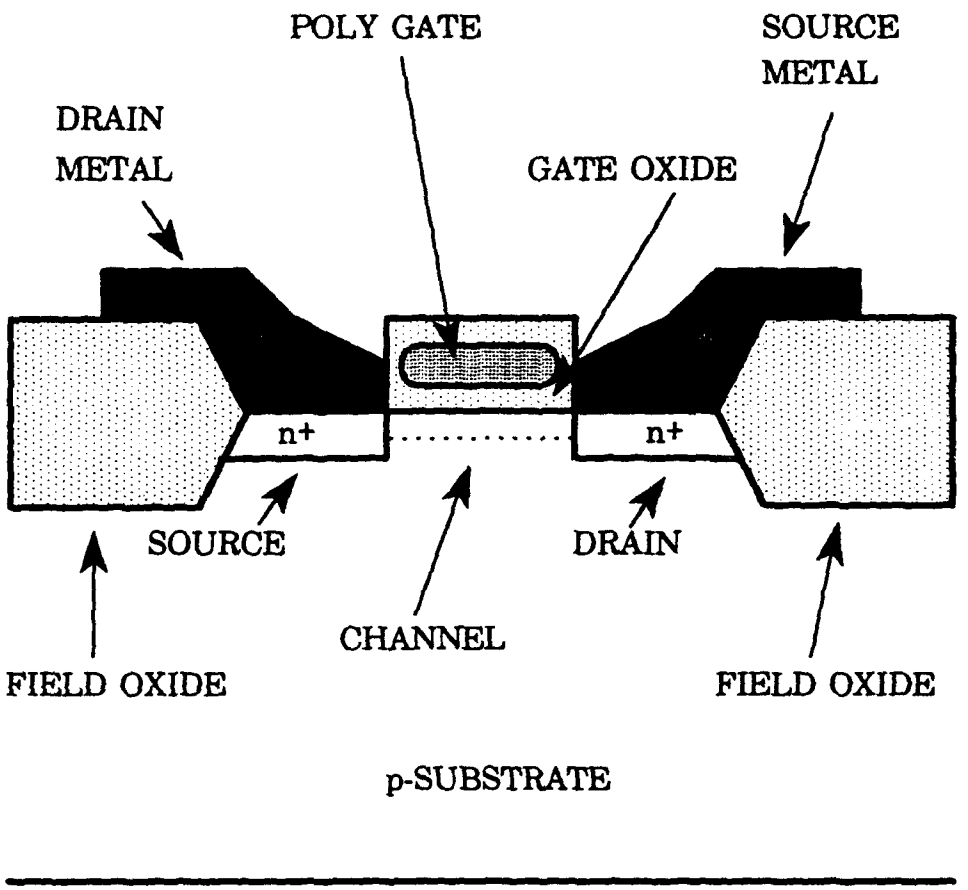


Figure 3.1 N-type Metal Oxide Silicon (NMOS) Transistor Illustration

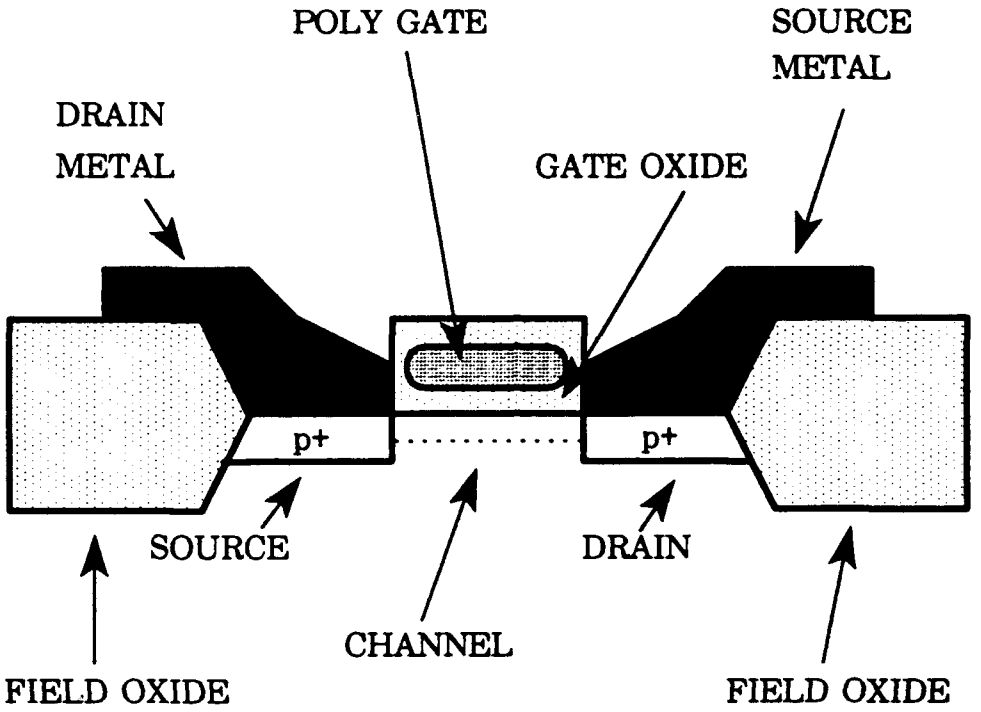


Figure 3.2 P-type Metal Oxide Silicon (PMOS) Transistor Illustration

Since the objective of the CMOS process is to provide the capability for NMOS transistors and PMOS transistors on the same substrate, it is clear from the discussion above that an additional feature is required. This additional feature is called a well. The well is an area in the substrate that is created by doping that area with a dopant that is opposite to the type used in the substrate. That is, a p-well process is one in which the wafer or substrate is n-type and then a well is added that is p-type. An n-well process is one in which the substrate is p-type and then a well is added that is n-type. Both of these processes allow for the manufacture of both PMOS and NMOS transistors in the same wafer. Figure 3.3 illustrates the layers and transistors as they would appear when using a p-well process. Figure 3.4 illustrates the layers and transistors as they would appear when using an n-well process.

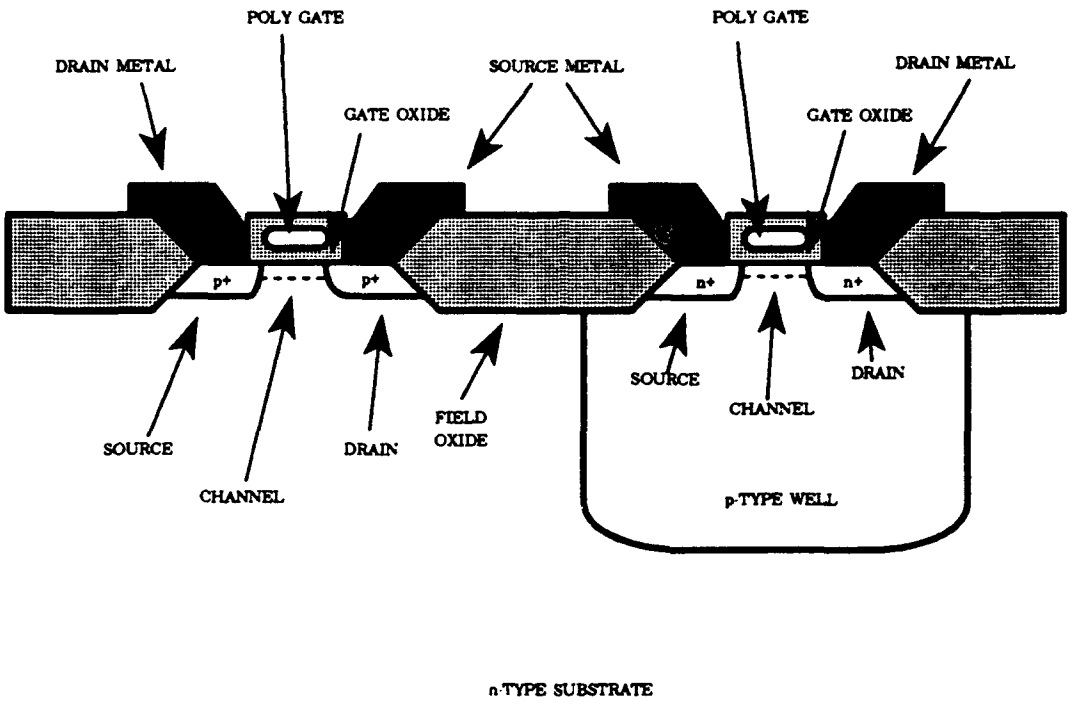


Figure 3.3 P-well CMOS Process Illustration

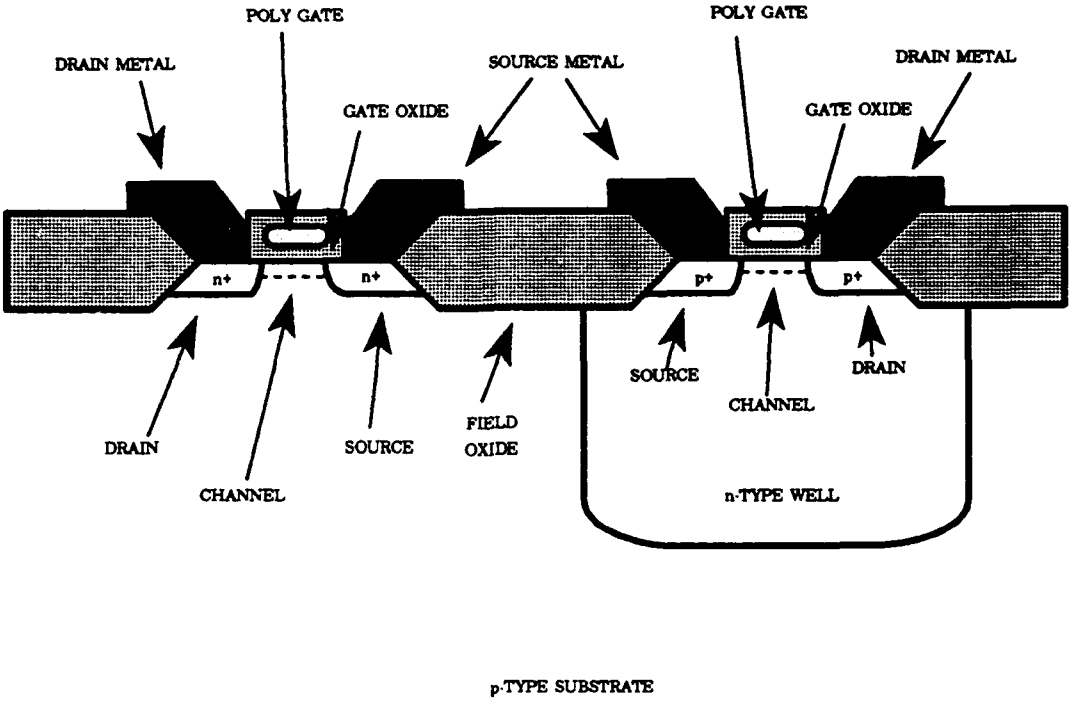


Figure 3.4 N-well CMOS Process Illustration

Another CMOS process that allows both PMOS and NMOS transistors on the same substrate is the twin tub process. This process is similar to those described above except that an epitaxial layer is produced above the substrate that is lightly doped. Then both p-wells and n-wells can be produced in this layer providing for the capability to produce NMOS and PMOS transistors. Figure 3.5 illustrates the layers and transistors as they would appear in a twin tub CMOS process.

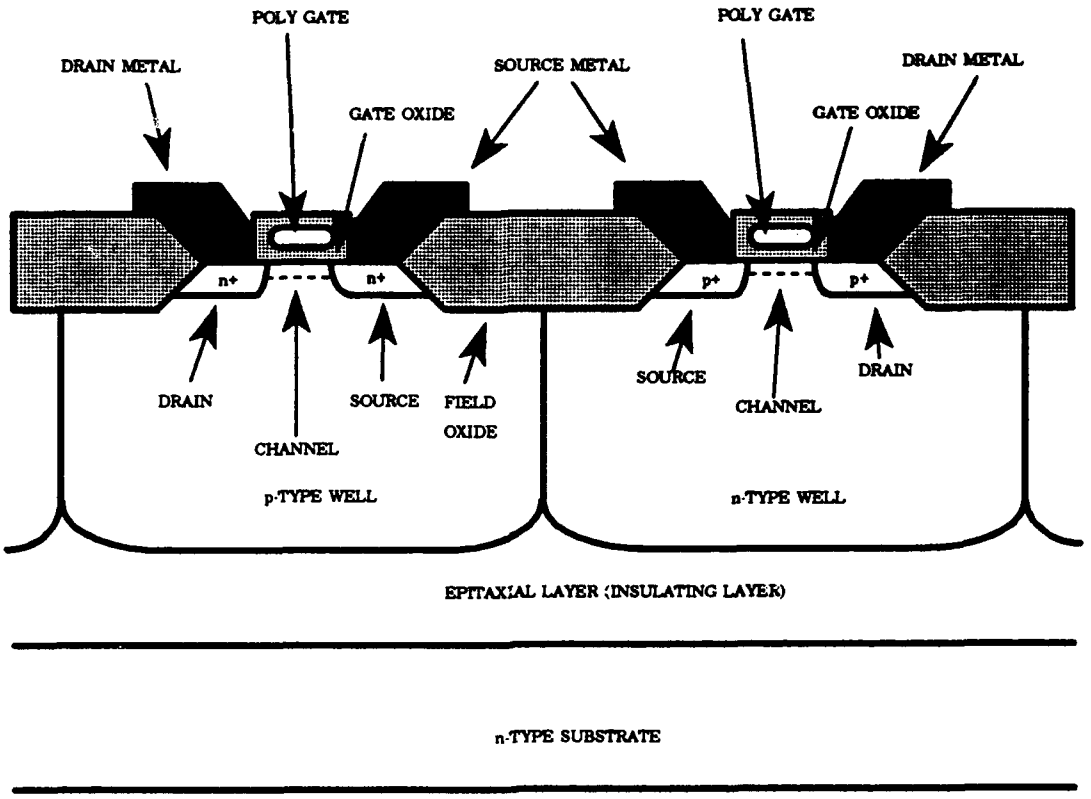


Figure 3.5 Twin Tub CMOS Process Illustration

Although the CMOS process provides much flexibility in circuit design, it does have some shortcomings. Probably the most troublesome drawback is "latch-up". The result of this effect is to provide a short between the most positive power supply and the most negative power supply, usually resulting in the destruction of the chip or at least a failed system requiring shutdown. Fortunately this characteristic is well understood now and can easily be controlled by design considerations. The method of controlling this problem is to provide a sufficient number of substrate contacts or well plugs. The purpose of the well plug is to bias the well to the power supply opposite the one that is biasing the native substrate. This creates a reverse bias on the well to substrate junction and prevents latch-up. These substrate contacts were illustrated in Figures 3.3 and 3.4. For a more detailed discussion of the CMOS process see Reference 9, pp. 32 - 98.

C. THE MOSIS PROCESS

In general, there are many different CMOS manufacturers that can provide a wide range of technologies to choose from. The technology is usually referred to by the length of the smallest transistor gate that can be produced with that process. Other variations on manufacturers include those that produce only a certain application microchip or those that provide some design flexibility in what is called a semi-custom microchip or those that provide the most design flexibility in what is called a fully custom microchip.

MOSIS was the manufacturing process available for the fabrication of the microchip designed in this thesis. The production line available was a 2 micron technology, full custom process. This means that the minimum sized transistor has a gate length of 2

microns and that the design could be anything that would not violate the technology design rules and would fit within the area of the microchip. Thus, this process allowed for the maximum amount of flexibility within the limits of the technology.

Specific features of the process are two layers of metalization called metal 1 (m1) and metal 2 (m2), a polysilicon (poly) layer used as the gate of transistors and for short interconnects, both NMOS and PMOS transistors, a p-type substrate with n-wells and for this design a maximum chip size of 2250 microns by 2220 microns. The maximum number of pins allowed was 40, in a dual in line package (dip).

IV. CMOS OPERATIONAL AMPLIFIER DESIGN

A. THE SEARCH FOR AN OPERATIONAL AMPLIFIER

Probably the most complicated and most important component needed to implement the composite operational amplifier circuits was the CMOS OA. Therefore, a significant amount of effort and research went into finding an existing design that would provide a general purpose amplifier with average characteristics that could be easily implemented in a VLSI design. Typical performance characteristics of a CMOS OA are unity gain bandwidth of several megahertz, open loop gain of ~10^4 and slew rate of ~5V/μs. Other important factors considered were stability and size. The primary indicator used for determining stability was phase margin. To ensure stability when placed in a closed loop feedback network the designs considered needed to provide 60° or more phase margin. The network to be implemented required eight operational amplifiers, thus it was important that the amplifier be small enough so that eight would fit on the available area and still leave enough room for switches, capacitors and a clocking circuit. With these requirements in mind three designs were tested and evaluated as possible amplifier designs.

Figure 4.1 through Figure 4.3 are circuit diagrams of the CMOS OAs considered for use on the microchip. Standard transistor symbols are used to represent the NMOS transistors and the PMOS transistors. Each of the three circuits was simulated on the transistor level using PSPICE and SPICE. The performance characteristics of the

fabrication process were used to establish the simulation parameters for the tests. The test results were compared and the three circuits were evaluated based on the simulation results and expected area that they would require when implemented. The following is a short description of each circuit.

The circuit in Figure 4.1 uses a total of thirteen transistors and a compensating capacitor. Transistors Q1, Q2, Q3, Q4 and Q5 are used to create a differential gain stage. Q1 and Q2 actually provide the differential pair and Q3 and Q4 are configured as load transistors. The bias current is established by Q5 and the bias point for Q5 is the result of the bias circuit created by Q11, Q12, and Q13. This particular bias arrangement was done so as to allow for dynamic Vss and Vdd , that is, the proper bias point was insensitive to changes in the voltages supplies. The differential gain stage is a differential input but a single ended output. The single ended output feeds into Q9 and Q6. Q9 in conjunction with Q10 provides level shifting and an additional gain stage. Q8 and the compensating capacitor provide feedback that maintains the stability of the amplifier. Q6 and Q7 provide a class-AB output stage, similar to a totem pole driver stage in bipolar technology. Some advantages of this circuit are internal compensation and an internal bias circuit which results in fewer external pins. It also can drive a larger load because of its dedicated output stage. An obvious disadvantage is the increased number of transistors. For a thorough analysis of the circuit see Ref. 9:pp 168 - 245.

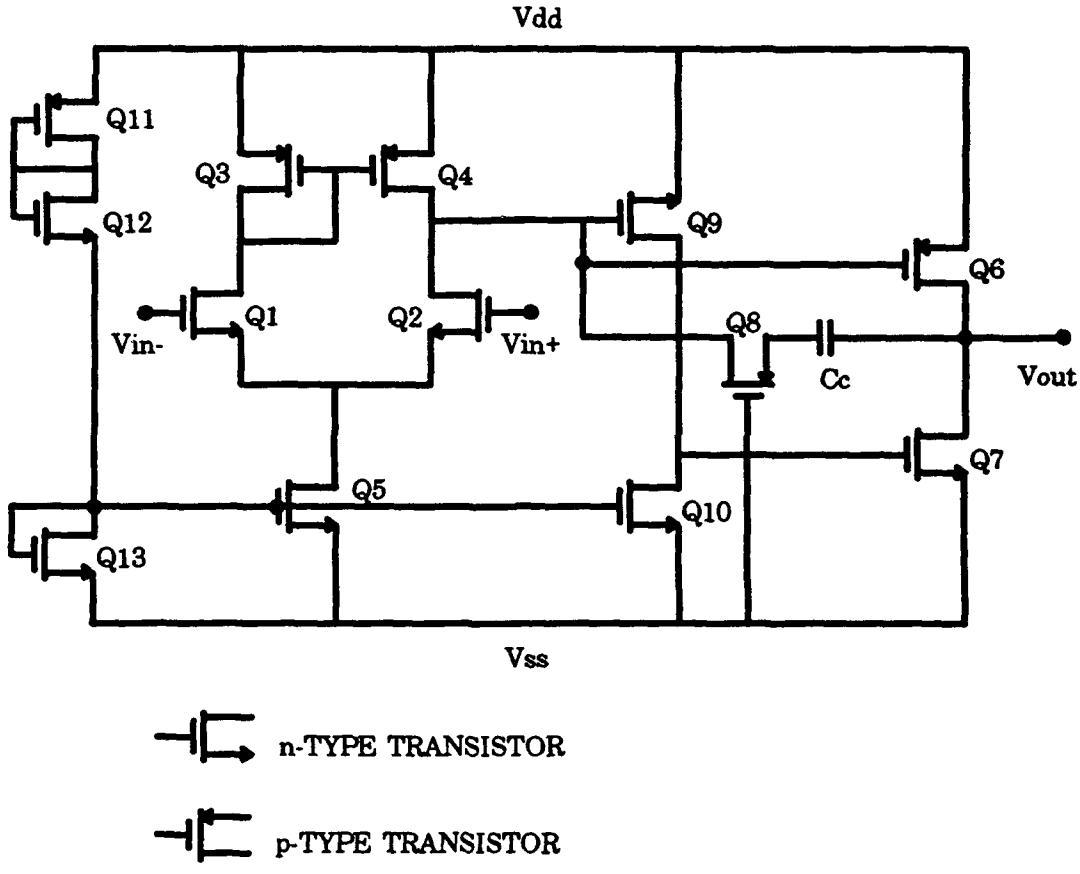


Figure 4.1 CMOS Operational Amplifier Design 1 Circuit Diagram

Figure 4.2 is the circuit diagram that represents another CMOS OA design. It is very similar in design to the operational amplifier in Figure 4.1. In fact, the differential input stage is identical and is also single ended on the output. Q6 and Q7 provide the level shifting, the second gain stage and the final output. Q8 and Cc provide feedback and are used to maintain stability. The bias circuit is established with Q9 and Q10. A clear advantage of this circuit is that it uses only 10 transistors; of course, this results in some trade offs. The bias circuit is now insensitive to variations in the positive voltage supply but, it is sensitive to variations in the negative voltage supply. Also, the second gain stage is driving the output and this prevents the amplifier from driving a very large load. For a complete analysis of this circuit see Ref. 9:pp 168 - 245.

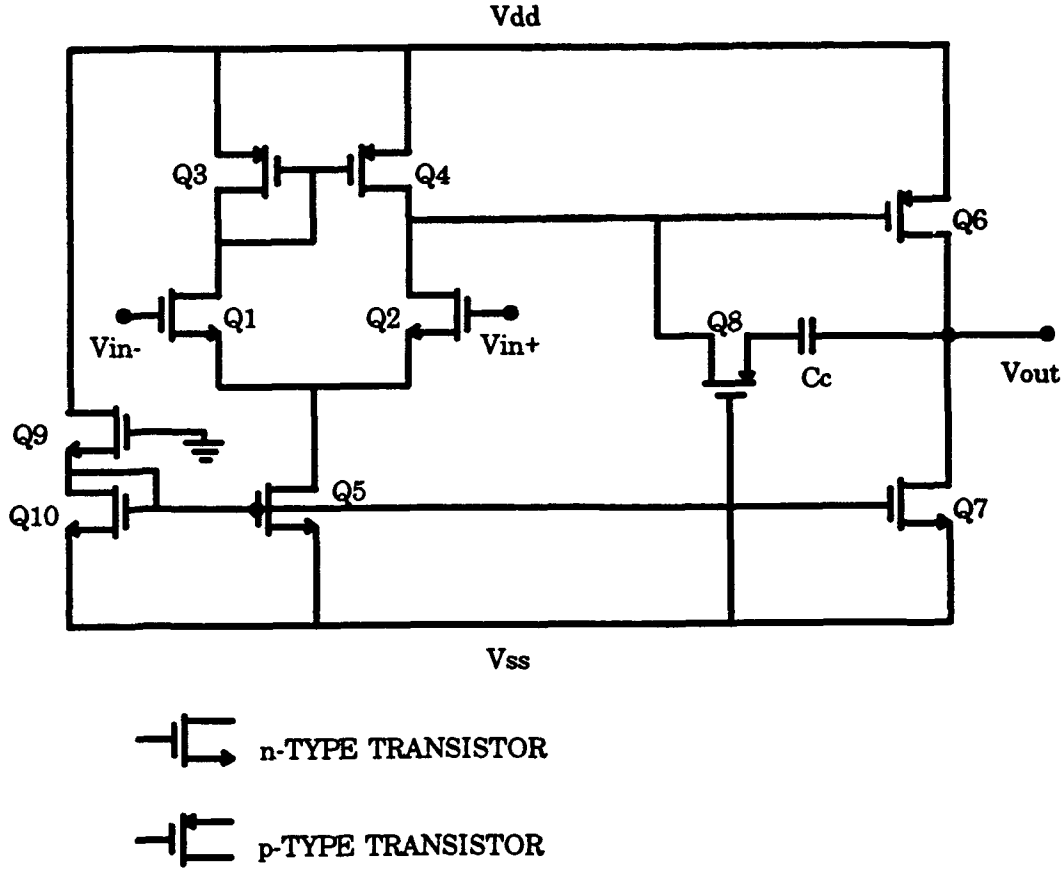


Figure 4.2 CMOS Operational Amplifier Design 2 Circuit Diagram

The circuit diagram in Figure 4.3 represents another CMOS OA that was considered for use in the microchip. This design is very similar to the two previous designs. It has a differential input implemented with Q1 and Q2. Q3, Q4 and Q8 are arranged to provide a load and to mirror the current established by Q5. The current through Q5 is set by Q6 when a load resistance is connected to Q6 at the Bias node. The differential stage has a single ended output that is input to the level shifting, gain stage implemented by Q9 and Q10. These transistors also provide the output stage. The Comp node provides a contact for a compensating capacitor which can be placed between the output and the input to the second gain stage. Some advantages to this design are the small number of transistors, the ability to select different bias points and the ability to adjust bandwidth, slew rate and stability by changing the compensating capacitor. Some disadvantages are the number of extra pins required as well as only being able to drive relatively small loads due to the output being taken directly from the secondary gain stage. For a more thorough discussion and analysis of this amplifier see Ref. 10 pp: 61 - 70.

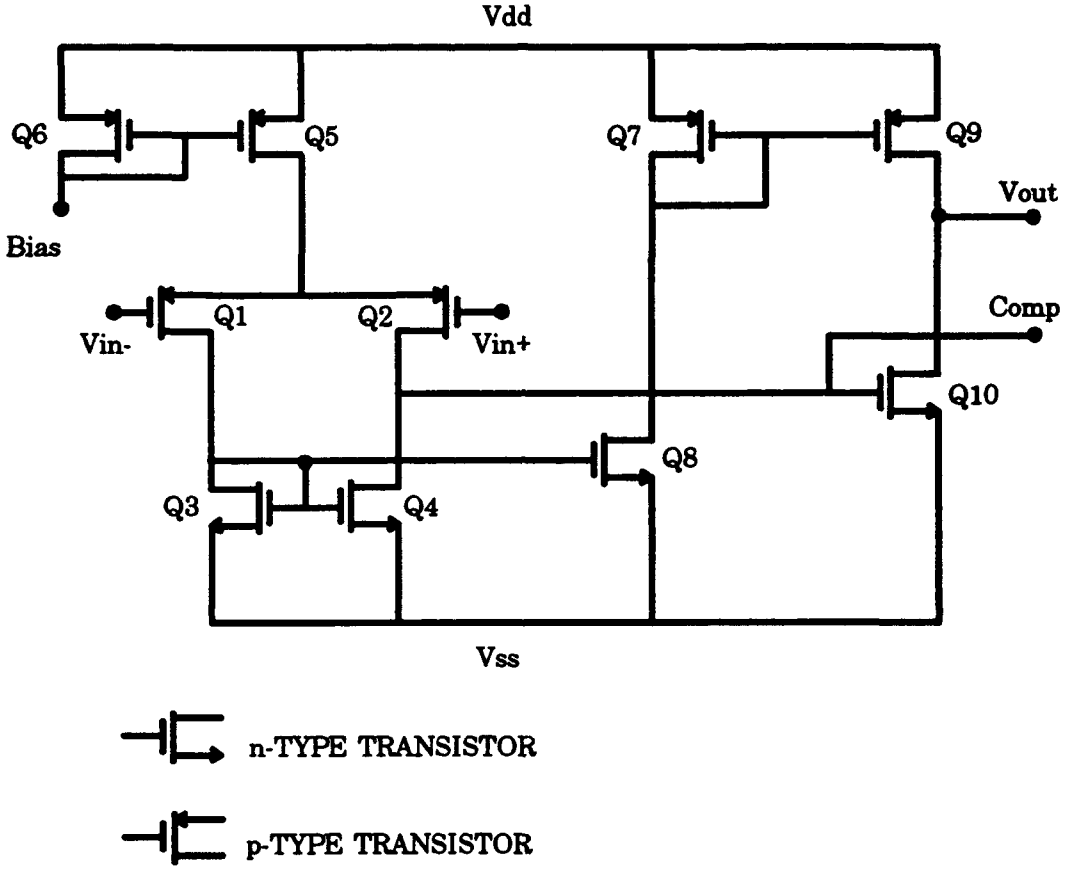


Figure 4.3 CMOS Operational Amplifier Design 3 Circuit Diagram

B. SELECTION OF A CMOS OPERATIONAL AMPLIFIER DESIGN

After carefully simulating the circuits described above, a comparison of their performance was made. Based on the simulation test results, it was decided to use the design presented in Figure 4.1. This circuit demonstrated the best overall performance of the three in terms of unity gain bandwidth, slew rate and phase margin. Of course, a disadvantage is that it requires 13 transistors while the other two designs require only 10 transistors each. In a following section this will be shown to be insignificant due the amount of area required for the internal compensating capacitor. The next step was to produce a circuit layout using a tool called MAGIC.

The layout of the operational amplifier can have significant effects on the performance parameters of the circuit. Affected parameters include rise time, overshoot, high frequency response, sensitivity to process variations and offset voltage. The amplifier arrangement should be such that the connecting line lengths are kept to a minimum. By doing this it will help to attain desired step response and high frequency response and reduce effects of input offset voltage. Other important factors to prevent input offset voltages are to arrange the input stage transistors close to each other as well as to their load transistors. Also, the input transistors should be in the same well and have identical geometries. These steps will help to reduce the offset voltages caused by process variations [Ref. 9:pp 513 - 524].

Since the amplifier geometry considerations are also compatible with layout considerations to maintain compact and efficient usage of available area, ensuring the

conditions stated above were implemented did not significantly complicate the design. With these factors in mind, the process of laying out the operational amplifier was started. The several variations of the implementation of the circuit in Figure 4.1 were designed and the layout was produced to compare the different geometries and to attempt to optimize all the layout considerations. Although a very good general pattern was established by performance criteria, there was a significant amount of just looking at the layout to envision possible alternatives that might improve the layout and optimize utilization of available chip area. Thus, the first design was definitely not the final design.

Eventually, a final design was decided on and Figure 4.4 shows the layout geometry. The transistor labels in the figure correspond to the labels used in Figure 4.1. It is clear from Figure 4.4 that the input stage transistors (Q1, Q2, Q3, Q4) are close to each other and the input and load pairs have identical geometries. Also, the input lines have no other signal lines crossing them and the input stage has good separation from the output stage (Q6, Q7). The bias circuit (Q11, Q12, Q13) is arranged along one side of the amplifier and determined the width of the layout. Only a portion of the compensating capacitor is shown in this figure, but, as will be shown later its dimensions determine the length of the OA layout.

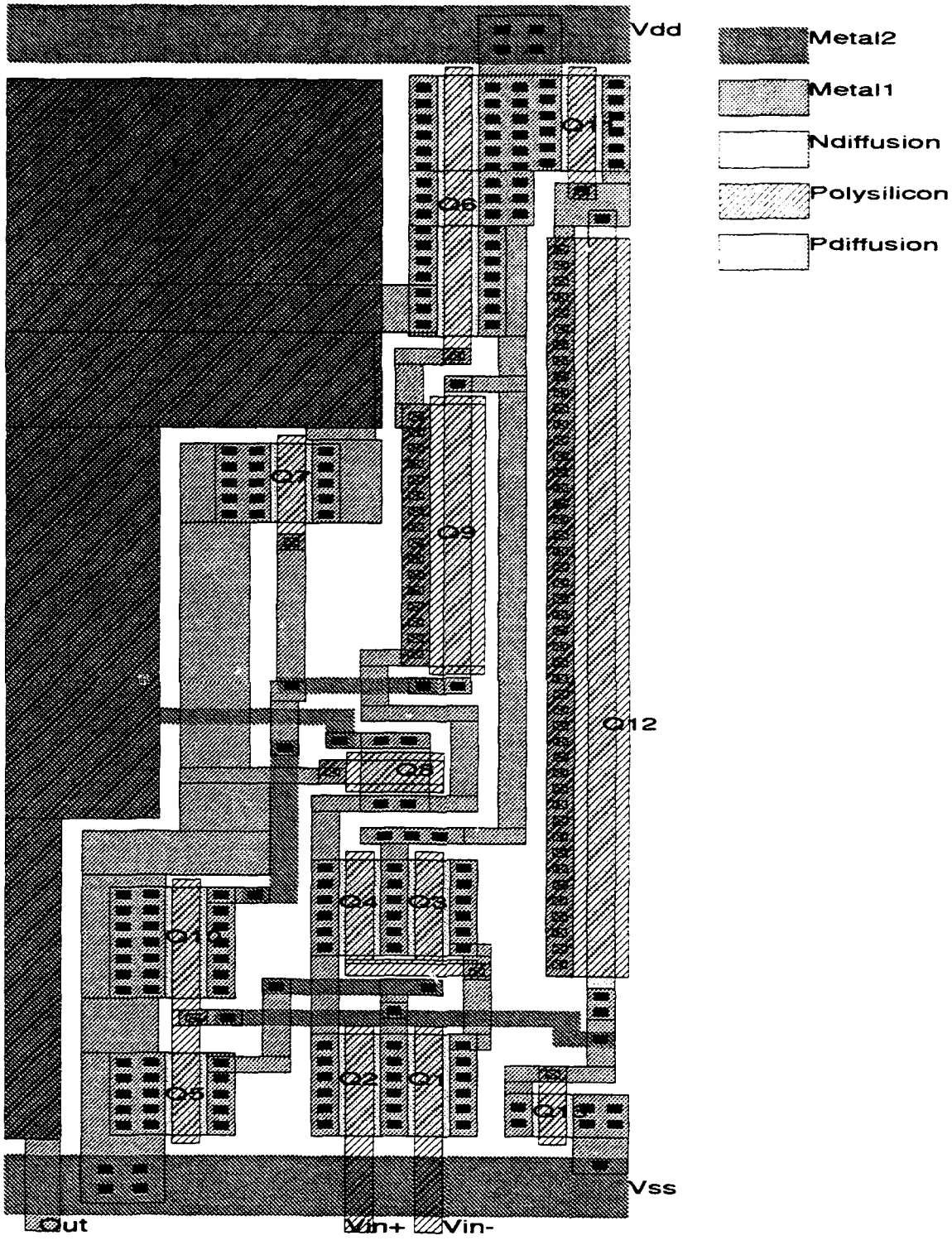


Figure 4.4 CMOS Operational Amplifier Layout Geometry

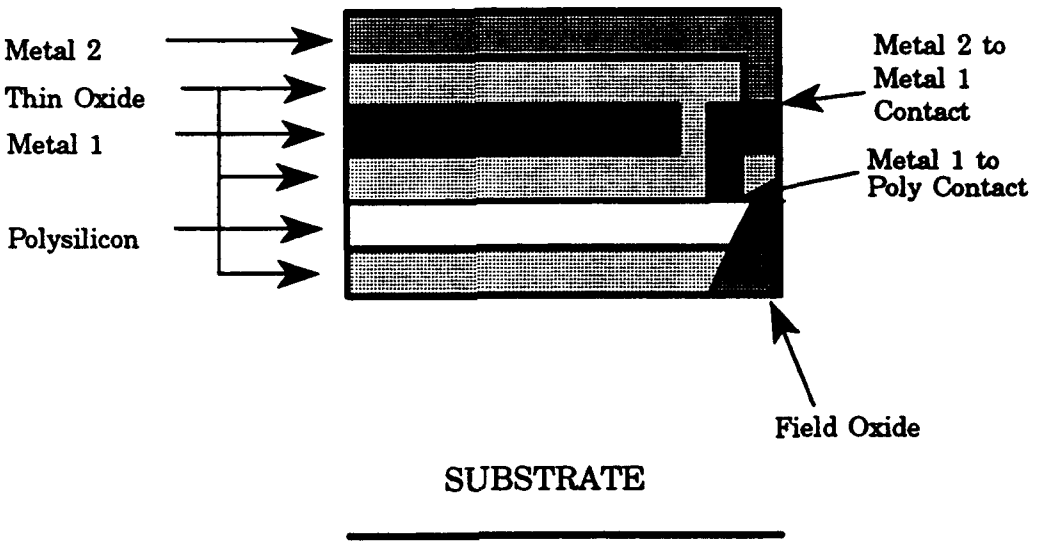
C. THE COMPENSATING CAPACITOR DESIGN

One of the difficulties in using a process optimized for digital design became apparent when trying to produce the desired size of compensating capacitor. There were no procedures for laying out a relatively large capacitance while at the same time using the smallest area possible. Therefore, a design had to be developed that would fill this need. It was decided that a parallel plate capacitor would be used. Equation 4.1 can be used to approximate the capacitance for a parallel plate design.

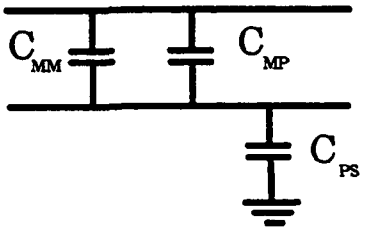
$$C = \frac{\epsilon}{t} A \quad , \quad \epsilon = \epsilon_r \epsilon_o \tag{4.1}$$

In Equation 4.1 C is the capacitance, ϵ is the dielectric constant of the insulating material between the plates, t is the insulator thickness and A is the area of the parallel plate capacitor. This model for approximating capacitance does not take into account the affects of fringe capacitance which can have a significant contribution to parallel plate capacitance. The effect of the fringing is to increase the capacitance. In the MOSIS process there are three layers of conductor which can be used to build parallel plate capacitors. Therefore, a three layer compensating capacitor was designed to provide the maximum amount of parallel plate capacitance using the least amount of area. Figure 4.5 illustrates the structure of this three layer construction. This design was based on the fact that the overall value of a capacitor is calculated by adding all the capacitances in parallel. By using this principle the amount of capacitance per unit area was approximately doubled. This effect is demonstrated in Figure 4.5 by the equivalent circuit

diagram. For this fabrication process, typical values of metal 1 to metal 2 capacitance was estimated to be $0.6X10^{-4}$ pF/μm^2 to $1.0X10^{-4}$ pF/μm^2. Estimated capacitance between metal 1 and polysilicon was $0.8X10^{-4}$ pF/μm^2 to $1.2X10^{-4}$ pF/μm^2 and estimated capacitance between polysilicon and the substrate was $0.8X10^{-4}$ pF/μm^2 to $1.2X10^{-4}$ pF/μm^2. From the circuit diagram and the estimates made of the capacitance, the compensating capacitor design should provide between $1.4X10^{-4}$ pF/μm^2 and $2.2X10^{-4}$ pF/μm^2. These values were used to determine the amount of area required to achieve a compensating capacitor value of 10 pF. This value was chosen as a typical value based on discussions in Reference 9:pp 168 - 245.



Circuit Diagram



Compensating Capacitance

$$C_C = C_{MM} + C_{MP}$$

C_{MM} Metal 2 to Metal 1 Capacitance

C_{MP} Metal 1 to Poly Capacitance

C_{PS} Poly to Substrate Capacitance

Figure 4.5 Three Layer Compensation Capacitor Illustration

The layout depicted in Figure 4.6 is the amplifier including the compensating capacitor. From this figure it is clear that the majority of layout area was used to create the compensating capacitor. Despite this, there was still sufficient area to implement the entire design. Although the compensating capacitors could have been taken off chip, this would have required 16 pins just for compensation and that would have prevented complete implementation of the design on the single microchip.

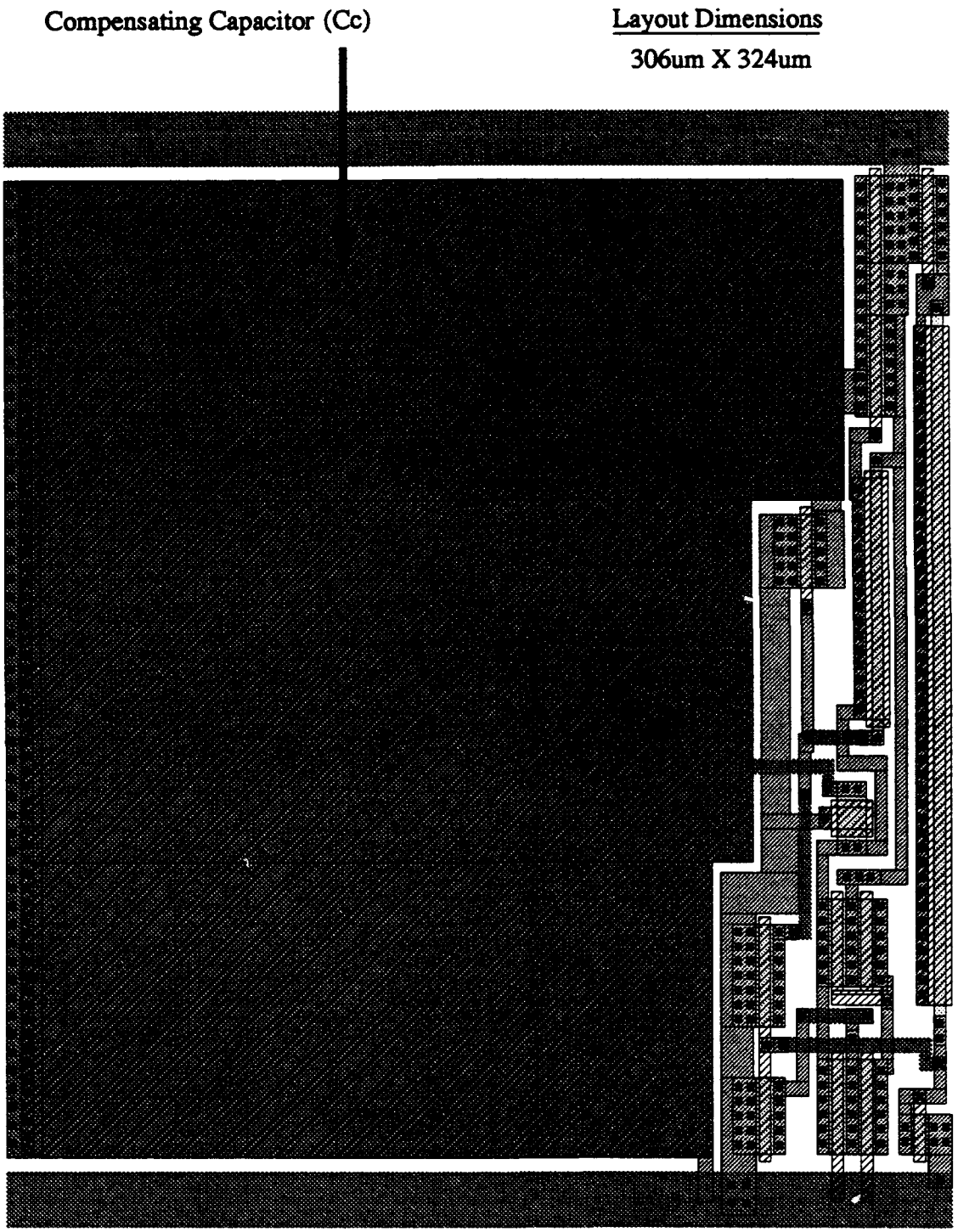


Figure 4.6 CMOS Operational Amplifier With Compensation Capacitor

D. TESTING AND ANALYSIS

The layout tool, MAGIC, provides the capability of extracting a SPICE file directly from the layout. This file is then filtered through another program, called ext2spice, that puts the file in the proper format for SPICE. Then the process parameters, power supplies and other necessary devices can be added to build a simulation of the circuit. The resulting SPICE file is in appendix A. The simulation was run to determine unity gain bandwidth, open loop gain, phase margin and slew rate. The plot contained in Figure 4.7 shows the magnitude and phase response and the plot in Figure 4.8 shows the slew rate. From these simulation results it can be easily shown that the open loop gain was ~10^4 V/V, the unity gain bandwidth was ~1.63 MHz and the phase margin was more than 80°. From Figure 4.8 the slew rate is ~6 V/μs. Therefore, this amplifier design met all of the requirements established in the first part of this chapter.

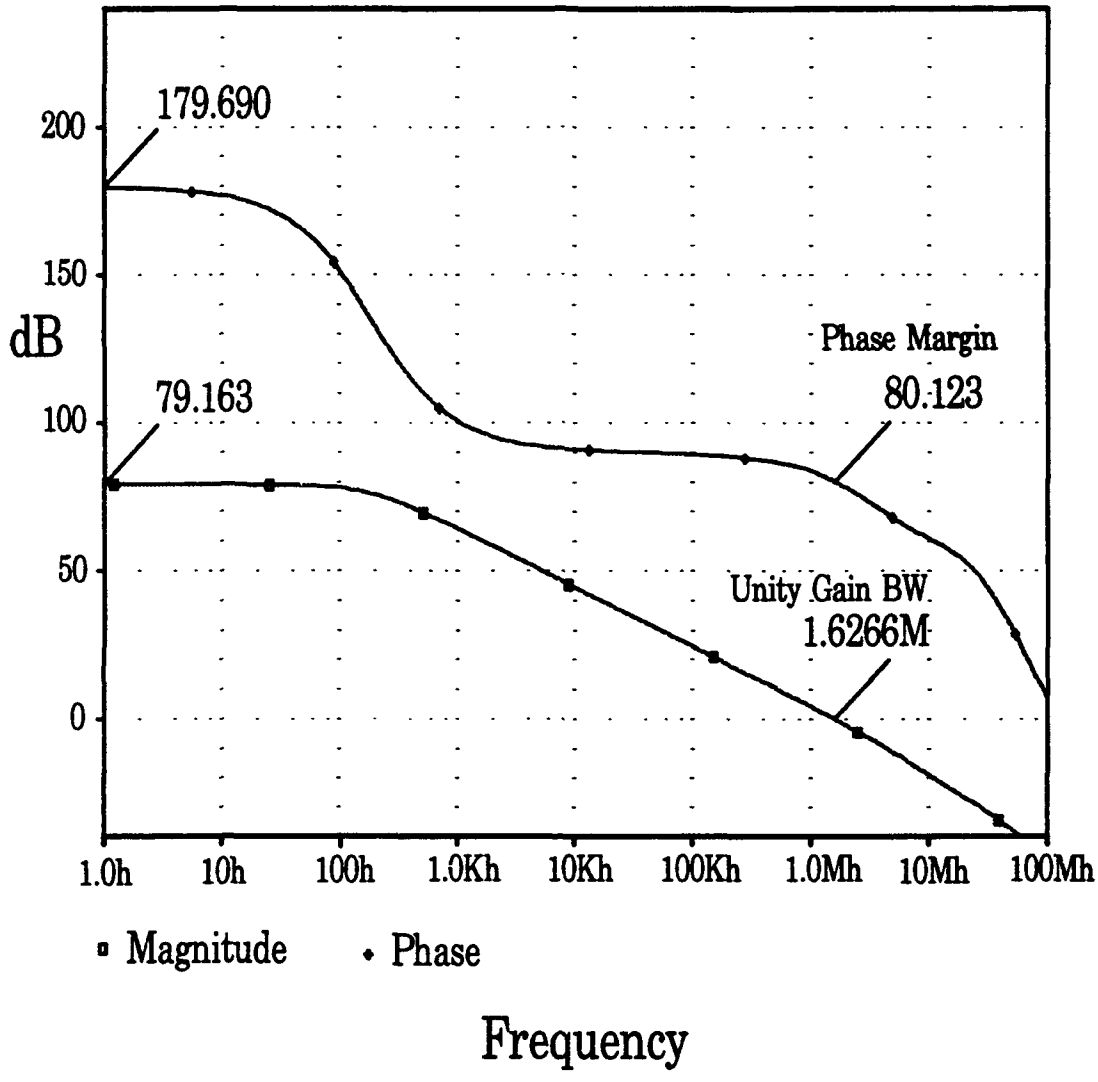


Figure 4.7 CMOS Amplifier Frequency Response

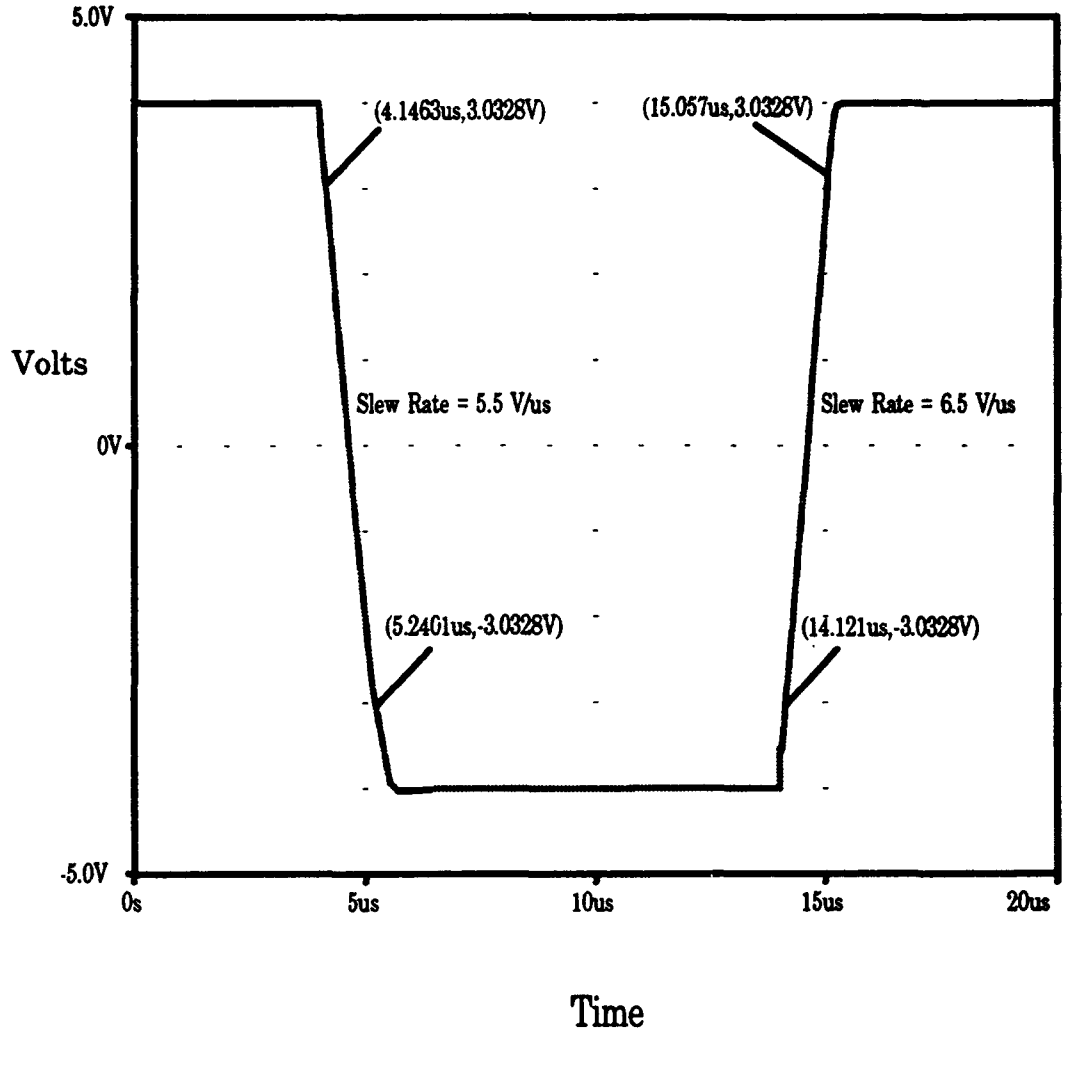


Figure 4.8 CMOS Amplifier Slew Rate

V. THE SWITCHED CAPACITOR AND TRANSMISSION GATE

A. DESIGN OF THE SWITCHED CAPACITOR

The most important design consideration for the switched capacitors was that the ratio of the capacitors, α, as depicted in Figure 1.1 through Figure 1.4, be as accurate as possible. The process being used does not provide a means to produce a very accurate capacitance value but, there are techniques that can be used to produce capacitor ratios that are very accurate. Accuracies of 0.1% or less can be achieved in the ratios of two capacitors in a VLSI design [Ref. 9:pp 474 - 482].

An extremely effective technique used to construct capacitor layouts that provide very accurate ratios and that are relatively insensitive to process variations is called a common centroid geometry [Ref. 9:pp 474 - 482]. This technique is based on a layout that uses a unit sized capacitor in the center of the design and then places the appropriate number of unit sized capacitors connected in parallel around the perimeter of the center capacitor. The value of the ratio is then determined by the number of capacitors surrounding the center capacitor. It is a very accurate ratio because the unit size capacitors are identical in layout area. If a fractional value is needed, one of the perimeter capacitors can be reduced or enlarged to obtain the exact ratio. The process of enlargement or reduction should be done in only one dimension, either width or length but not both. Figure 5.1 depicts the common centroid geometry.

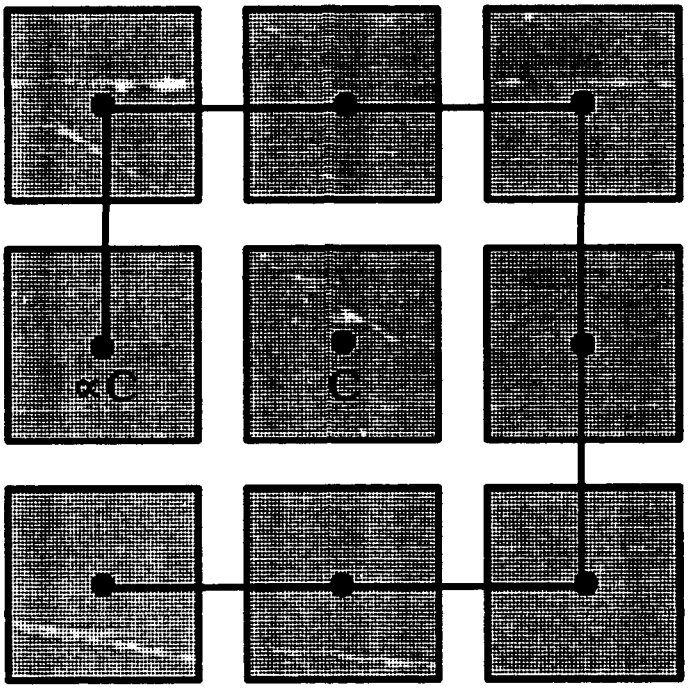


Figure 5.1 Switched Capacitor Centroid Geometry

The next step was to determine the size of the unit capacitor for implementation on the VLSI circuit. A primary consideration was the amount of layout required. This constraint resulted in the decision to construct a unit capacitor that was approximately 1pF in value. Again, it is important to remember that the accuracy of the capacitance is not very good. The actual value could fall between 0.5pF and 2pF. This design employed a parallel plate capacitor, C_p, using only metal 1 and metal 2 to form the plates. Figure 5.2 illustrates the design and also shows the parasitic capacitance, C_b , to the substrate and the parasitic capacitance, C_m , from the metal routing that is created. As was shown in Ref. 8:pp 43 - 68, this capacitance does not degrade the performance of the circuit due to the stray insensitive topologies used.

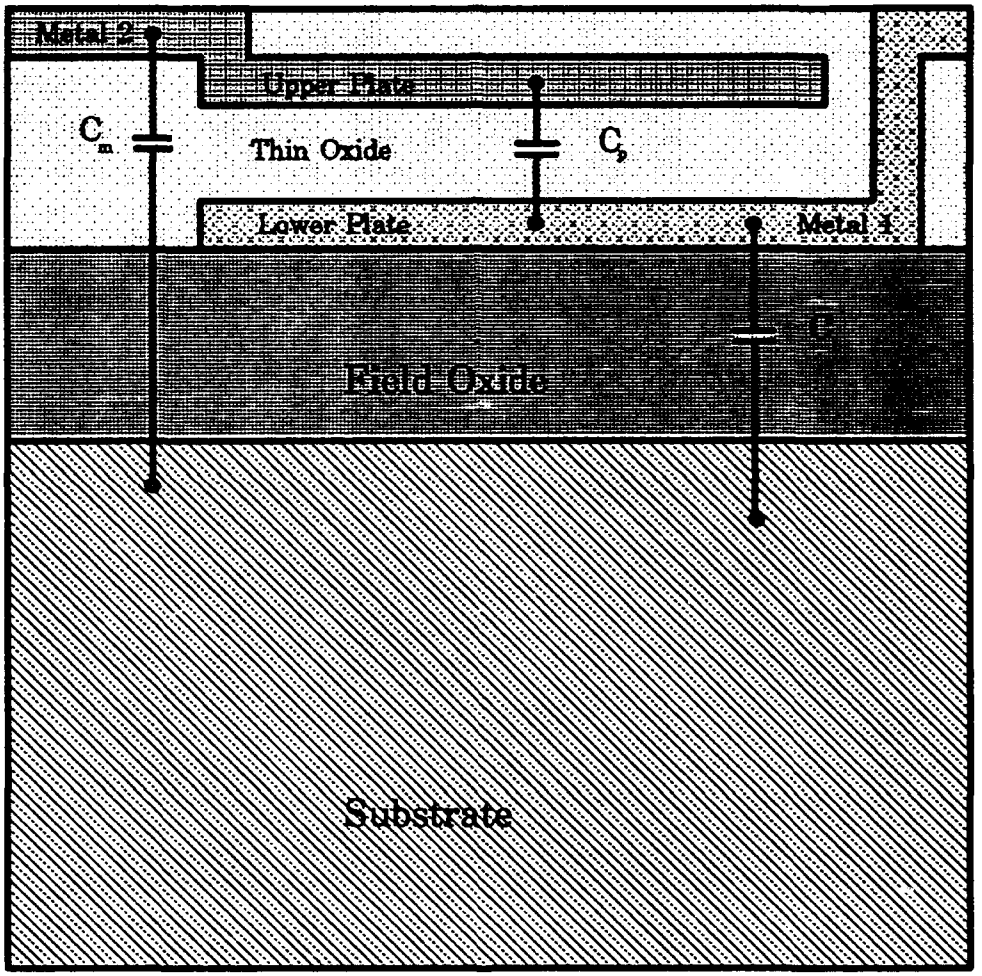


Figure 5.2 Parallel Plate Capacitor Illustration

The final step was to implement the common centroid geometry with the proper ratio, $\alpha = 6.11$, which was determined by the closed loop gain, $k = 100$, from Ref. 8:pp 7 - 19. This design was for a maximally flat magnitude response for this particular closed loop gain value. Using this fact the design layout in Figure 5.3 was produced. This figure shows the unit capacitor in the center and the six perimeter capacitors, one of which is slightly enlarged to produce the exact ratio.

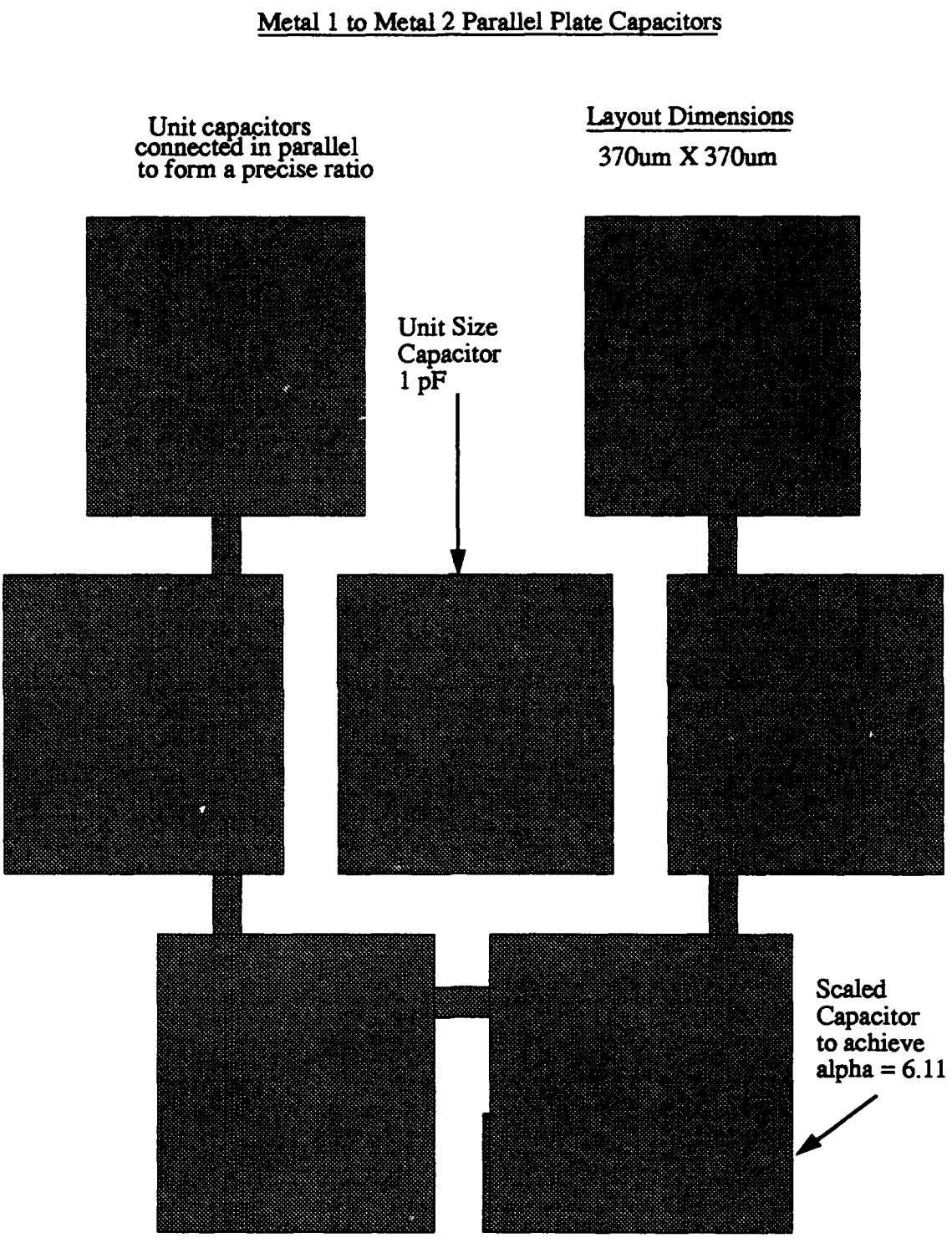


Figure 5.3 Switched Capacitor Layout Geometry

B. DESIGN OF THE TRANSMISSION GATE

The transmission gate or pass gate acts as a switch in the CMOS technology. It is designed using one PMOS transistor and one NMOS transistor with the drains connected together and with the sources connected together. When a positive voltage, greater than the threshold voltage, is applied to the gate of the NMOS transistor and a negative voltage, greater than the threshold voltage, is applied to the gate of the PMOS transistor, the transmission gate is on. This is equivalent to closing a switch. When the gate voltages are reversed the transistors are turned off which is equivalent to opening a switch. When the switch is closed the input signal should pass through the gate unchanged and when the switch is open no signal should pass through the gate. Although this is the ideal case there are some nonideal characteristics that must be considered.

Nonideal characteristics that can affect the performance of the circuit are the parasitic capacitances associated with transistors and the on-channel resistance of the transmission gate. The parasitic capacitances have already had their effects minimized by the use of the stray insensitive topology. The on-channel resistance for a minimum size transmission gate layout is on the order of several kilo-ohms. Clearly this amount of resistance will have a significant affect on the signal that is being passed. Therefore, a major design consideration was to reduce the on-channel resistance. Equation 5.1 shows the relation of the on-channel resistance to the dimensions of the transistors. R_c is the on-channel resistance and k is determined by: μ, the surface mobility of the majority carrier; t_{ox}, the thickness of the oxide or insulating layer; ε_o and ε_r, the dielectric constant

$$R_c = k\left(\frac{L}{W}\right), \qquad k = \frac{1}{\mu\left(\frac{\epsilon_o \epsilon_r}{t_{ox}}\right)(V_{gs}-V_t)} \tag{5.1}$$

of the insulating laye; V_t, the threshold voltage of the transistor and V_{gs}, the gate to source voltage of the transistor. L and W are the length and width of the transistor gate. The only parameters in the process that can be controlled by the designer are the width and length of the transistor. From Equation 5.1, it is apparent that if the ratio of the length to width of the transistor is reduced the on-channel resistance will decrease. There are two ways to reduce the ratio. One way is to make the length as small as possible and the second way is to increase the width of the transistor gate. Both of these methods were used to decrease the on-channel resistance of the transmission gate.

After testing several designs, the effect of continuing to increase the gate width did not reduce the on-channel resistance as much as when two transmission gate were connected in parallel. That is, if a transistor with a gate width of 80μm was compared to two transistors in parallel with gate widths of 40μm, the parallel configuration had between 20% and 30% less on-channel resistance. Therefore, this technique was used in the design of the transmission gate to reduce the on-channel resistance while using the least amount of area. Figure 5.4 shows the layout geometry of the transmission gate. The following plot in Figure 5.5 illustrates the simulation of on-channel resistance verses signal voltage for the transmission gate shown in Figure 5.4.

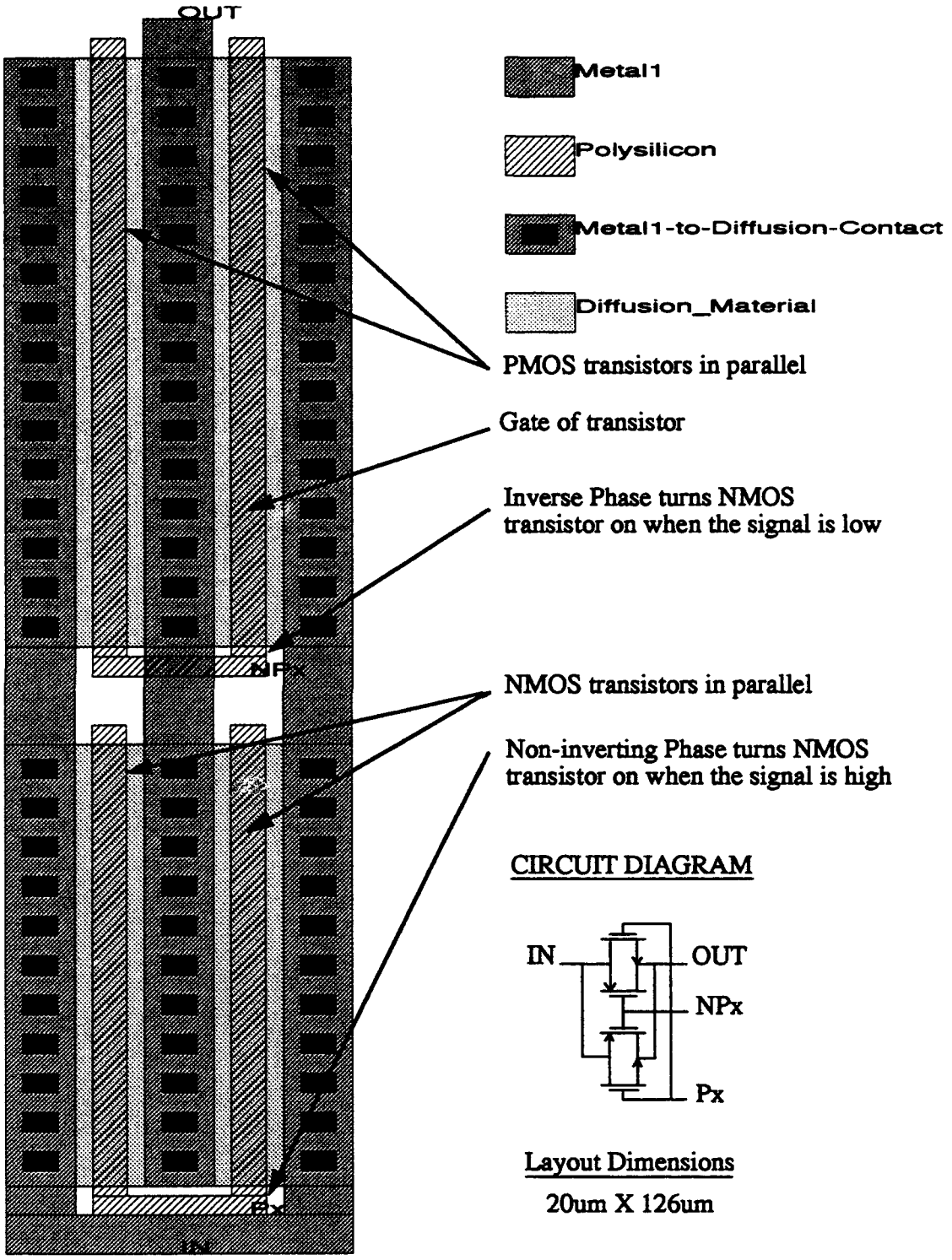


Figure 5.4 Transmission Gate Layout Geometry

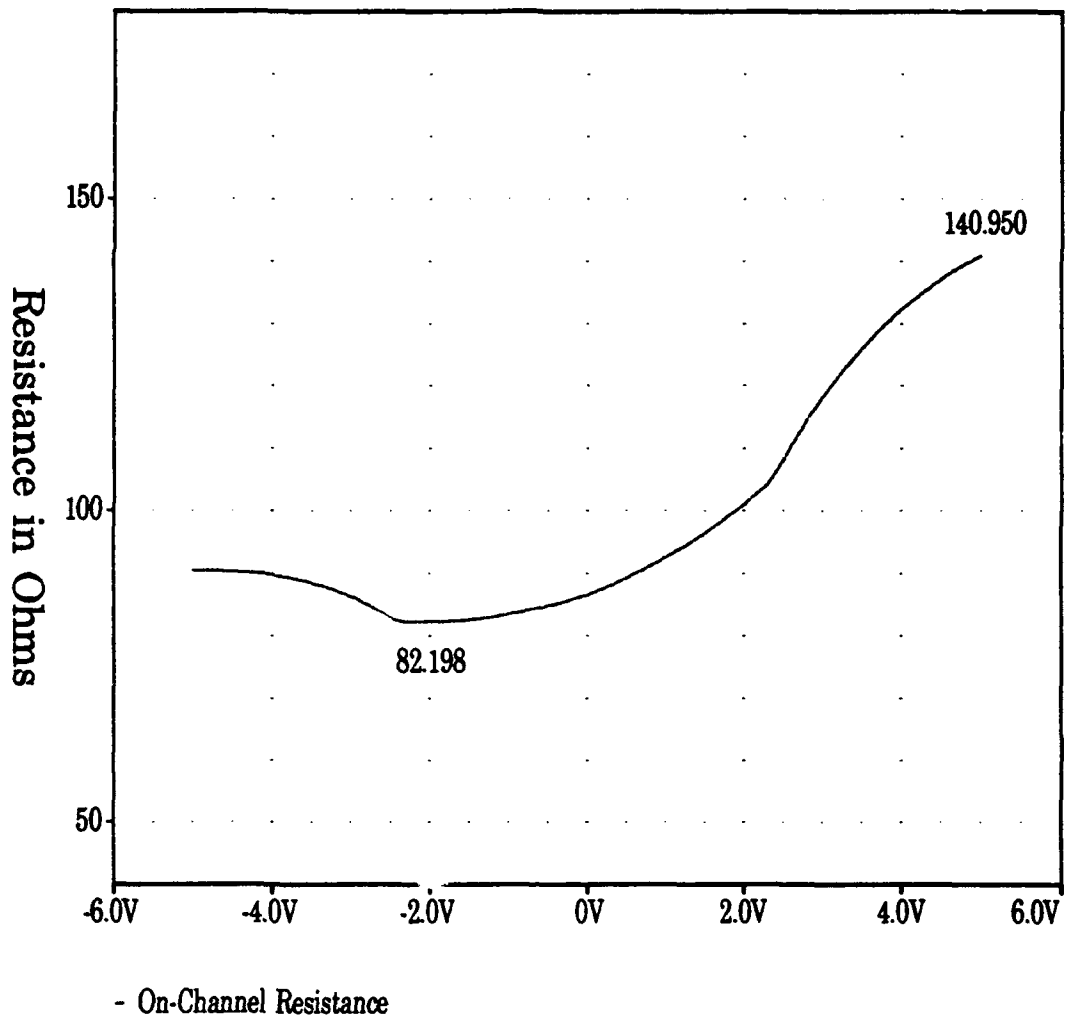


Figure 5.5 Transmission Gate On-Channel Resistance

From the graph in Figure 5.5 it can be seen that the on-channel resistance the transmission gate varies between 82Ω and 141Ω but, the on-channel resistance is less than 100Ω for most of the range of the signal change. The signal voltage was only simulated from -5 volts to +5 volts because that is the maximum signal that could be applied to this circuit. In actual applications the voltages will be much smaller in magnitude.

VI. THE TWO PHASE NON-OVERLAPPING CLOCK

A. THE PURPOSE OF THE CLOCK

The need for the two phase non-overlapping clock comes from the use of switched capacitors in the circuit design. The transmission gates discussed in Chapter V requires a signal to control when and for how long the switch is opened and closed. Also, the nodes that are connected to the transmission gate are switched alternately between two different portions of the circuit depending on the circuit topology. There is also a need for a small delay between one switch closing and one switch opening. This delay is provided by the two phase non-overlapping clock circuit.

In order to switch the transistors of the transmission gate on and off, the inverse of each phase is also required. The transmission gate that is controlled by the even phase signal also requires the inverse of that signal and the transmission gate that is controlled by the odd phase signal also requires the inverse of that signal. This is necessary because the signal that turns off the NMOS transistor will not turn off the PMOS transistor in the same transmission gate. The PMOS transistor needs a signal that is the inverse of the control signal used in the NMOS transistor. The clock circuit that is used provides access to both phases of the signals; therefore, no additional components are needed for proper switching.

B. DESIGN OF THE TWO PHASE NON-OVERLAPPING CLOCK

There are several designs available that will provide the clocking signals used in switched capacitor circuits. The two phase non-overlapping clock is built using a latch and then placing multiple inverters in the feedback path [Ref. 9:pp 516 - 518]. Figure 6.1 shows the circuit diagram and the waveforms that are produced by this circuit. The non-overlapping phase gap is the result of the addition of the gate delay of the multiple series connected inverters. The non-overlapping phases illustrated show a relatively large gap between the transitions in the signal. This large gap was done only to demonstrate that the signals are non-overlapping. The gap between phases produced by the circuit are actually very small (i.e., nanosecond range).

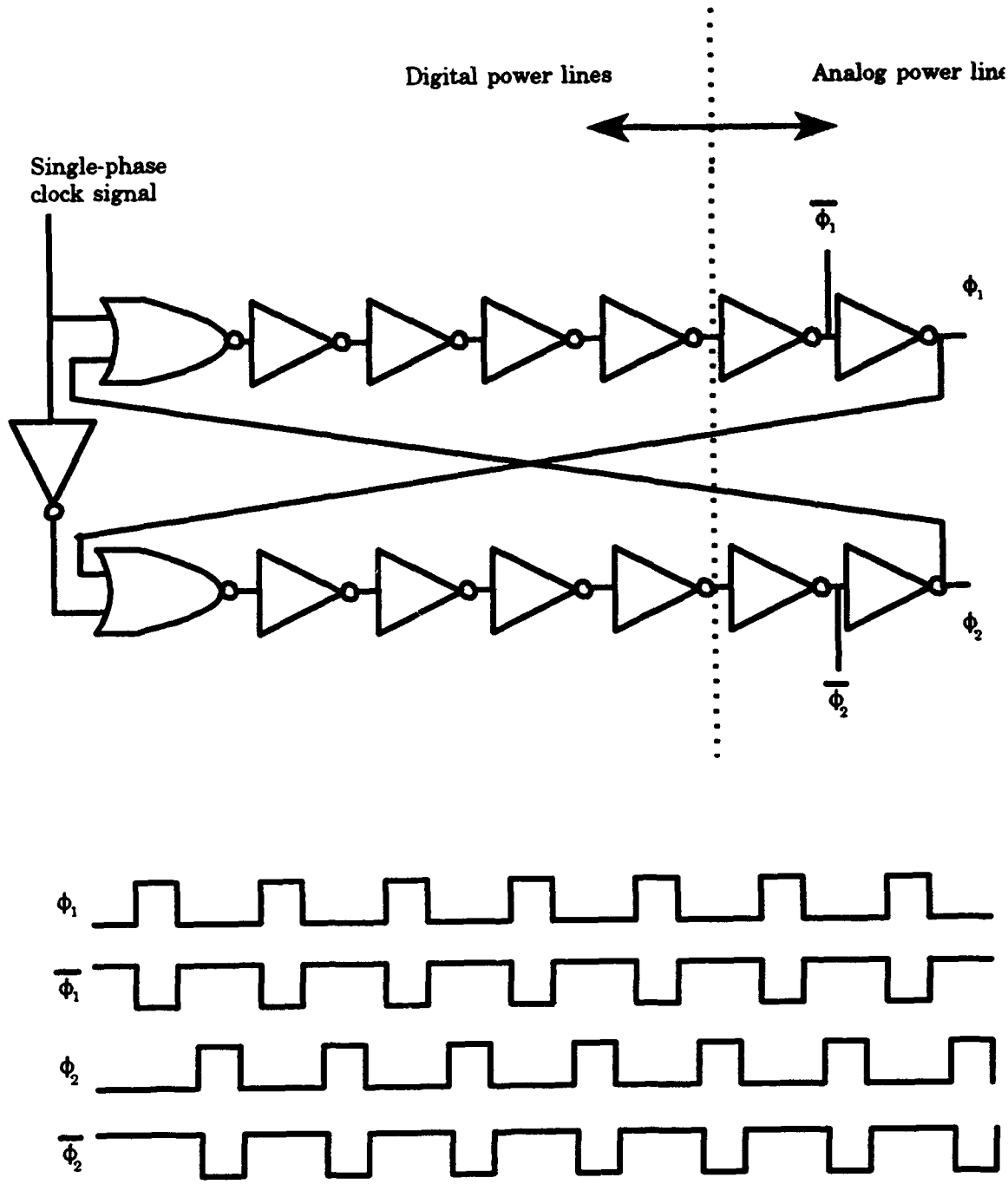


Figure 6.1 Two Phase Non-overlapping Clock Circuit Diagram

Figure 6.1 shows that the circuit was divided into two section for power distribution. The purpose of separating the digital power lines and the analog power lines was to try to isolate the large current spikes in the digital power lines from the analog power lines thus, preventing noise from feeding into the analog portion of the circuit from the digital portion of the circuit. This design consideration required providing separate pins for analog power and for digital power. This will be illustrated further in chapter VII.

One of the characteristics of the digital circuit that needed to be considered was the fan out of the circuit. A common rule of thumb is that the fan out of a single CMOS stage should not exceed eight. That is, the signal driver stages for the two phases and their inverses should drive only eight similar size transistors. The circuit being built utilized 32 transmission gates. Half of the transmission gates were driven by the odd phase clock signal and the other half of the transmission gates were driven by the even phase clock signal. Therefore, it was decided to use two clock circuits in the design so that each phase would be driving a maximum of eight transmission gates. This rule of thumb assumes that the driver is similar in size to the transistors being driven, thus, the stages of inverters were increased from the minimum size allowed by the technology in the first stage, to four times the minimum size in the final driver stage. Figure 6.2 shows the transistor level circuit diagram of the clock, while Figure 6.3 illustrates the layout geometry of the two phase non-overlapping clock circuit.

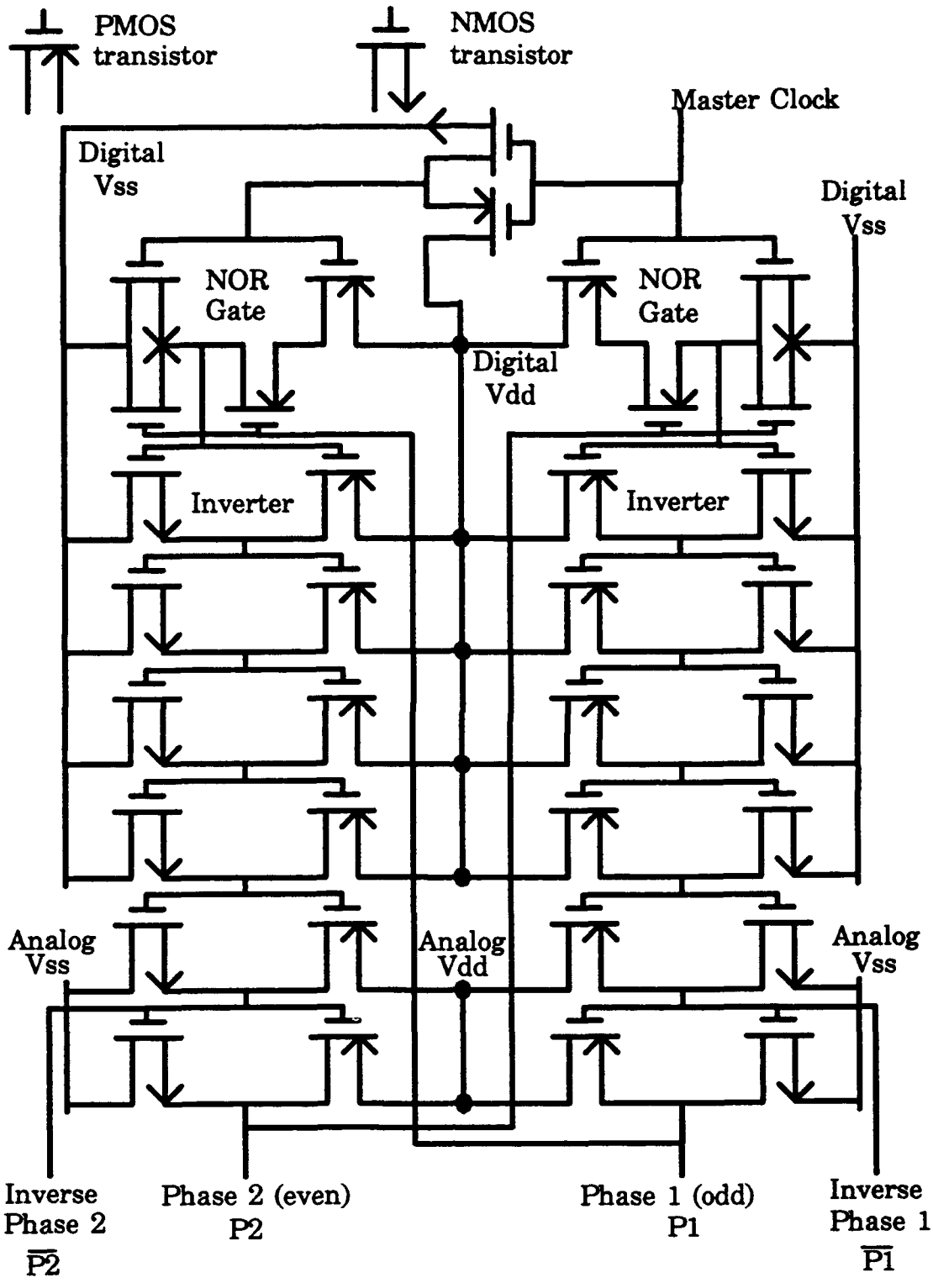


Figure 6.2 Two Phase Non-overlapping Clock Transistor Level Circuit Diagram

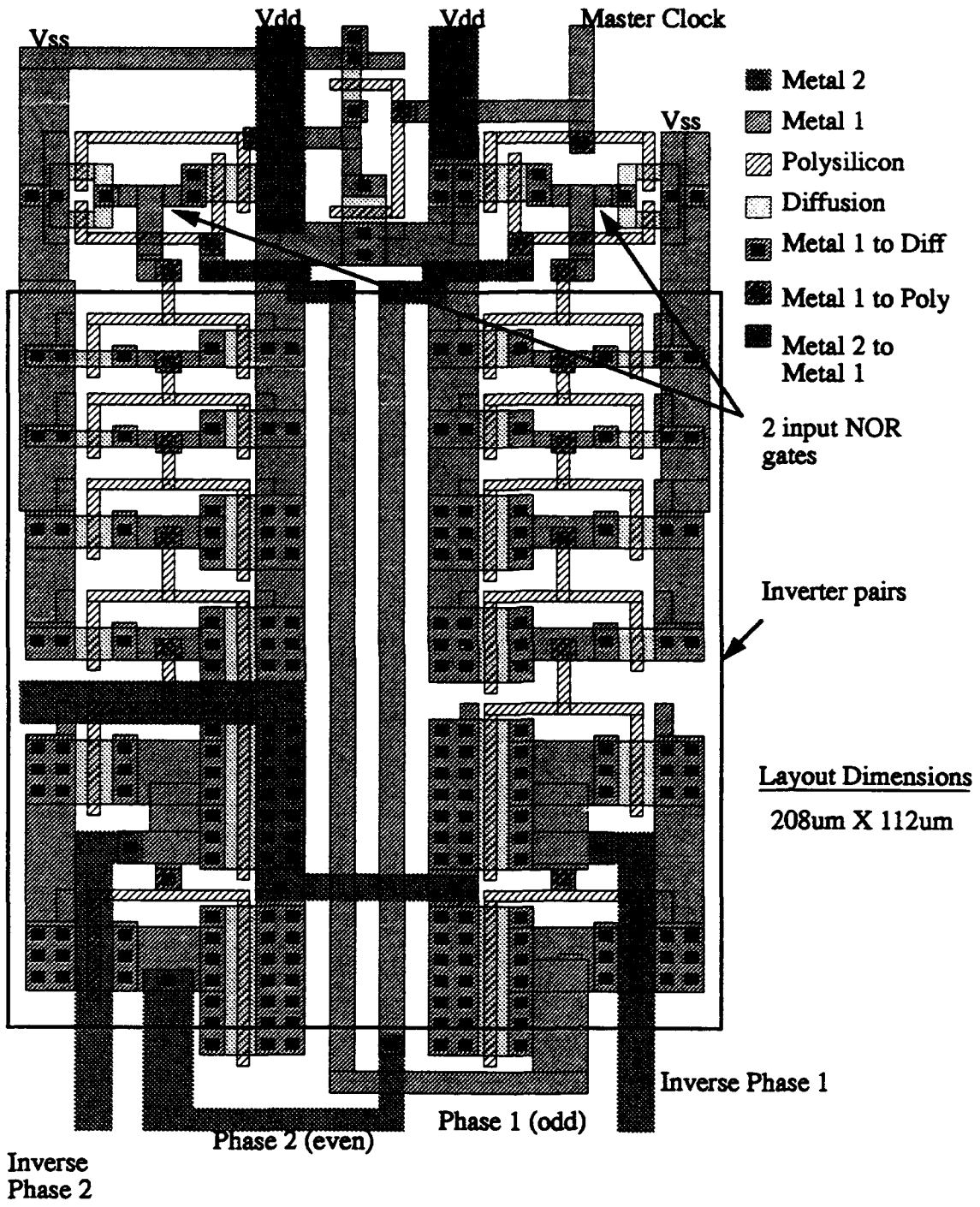
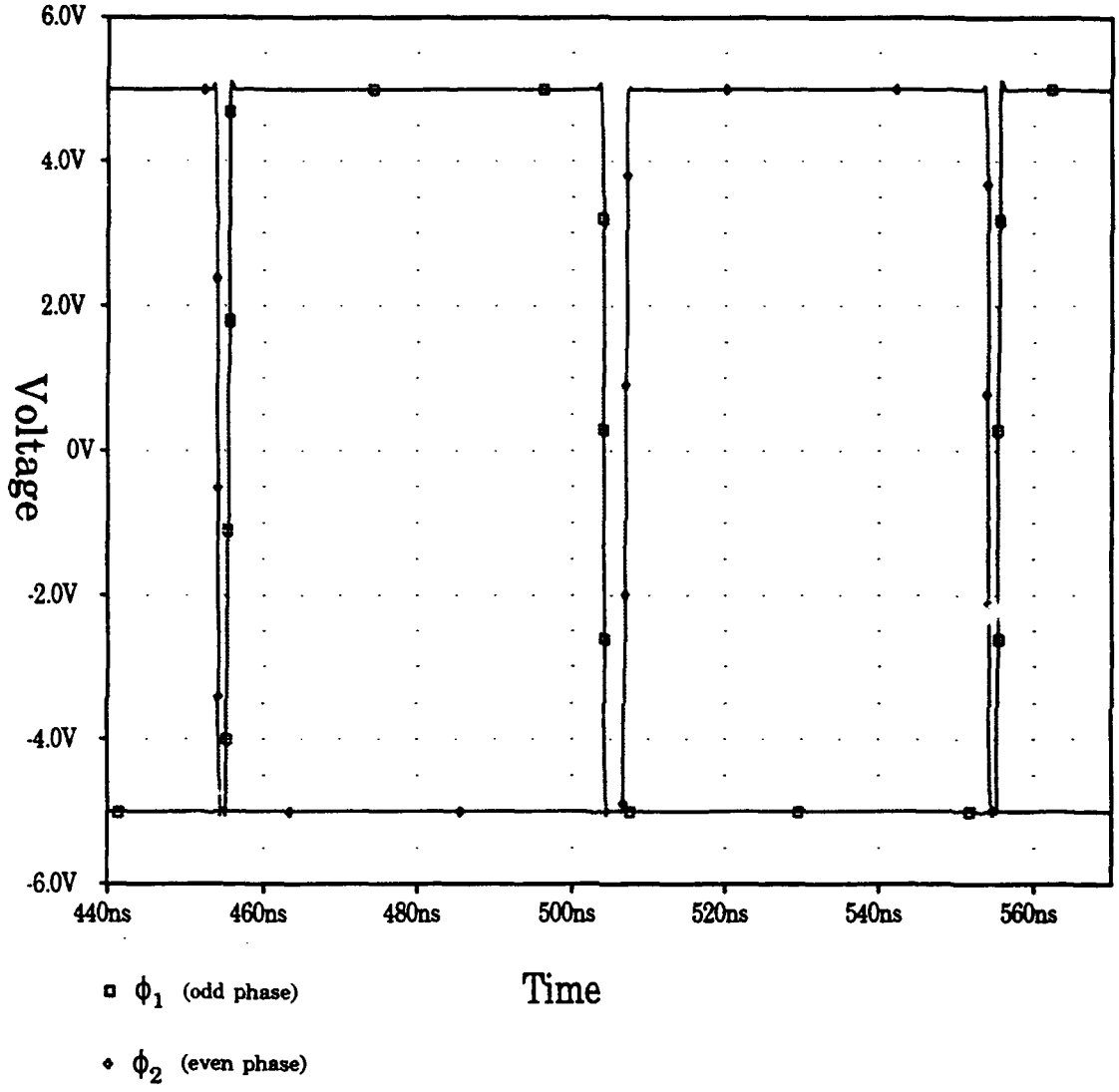


Figure 6.3 Two Phase Non-overlapping Clock Layout Geometry

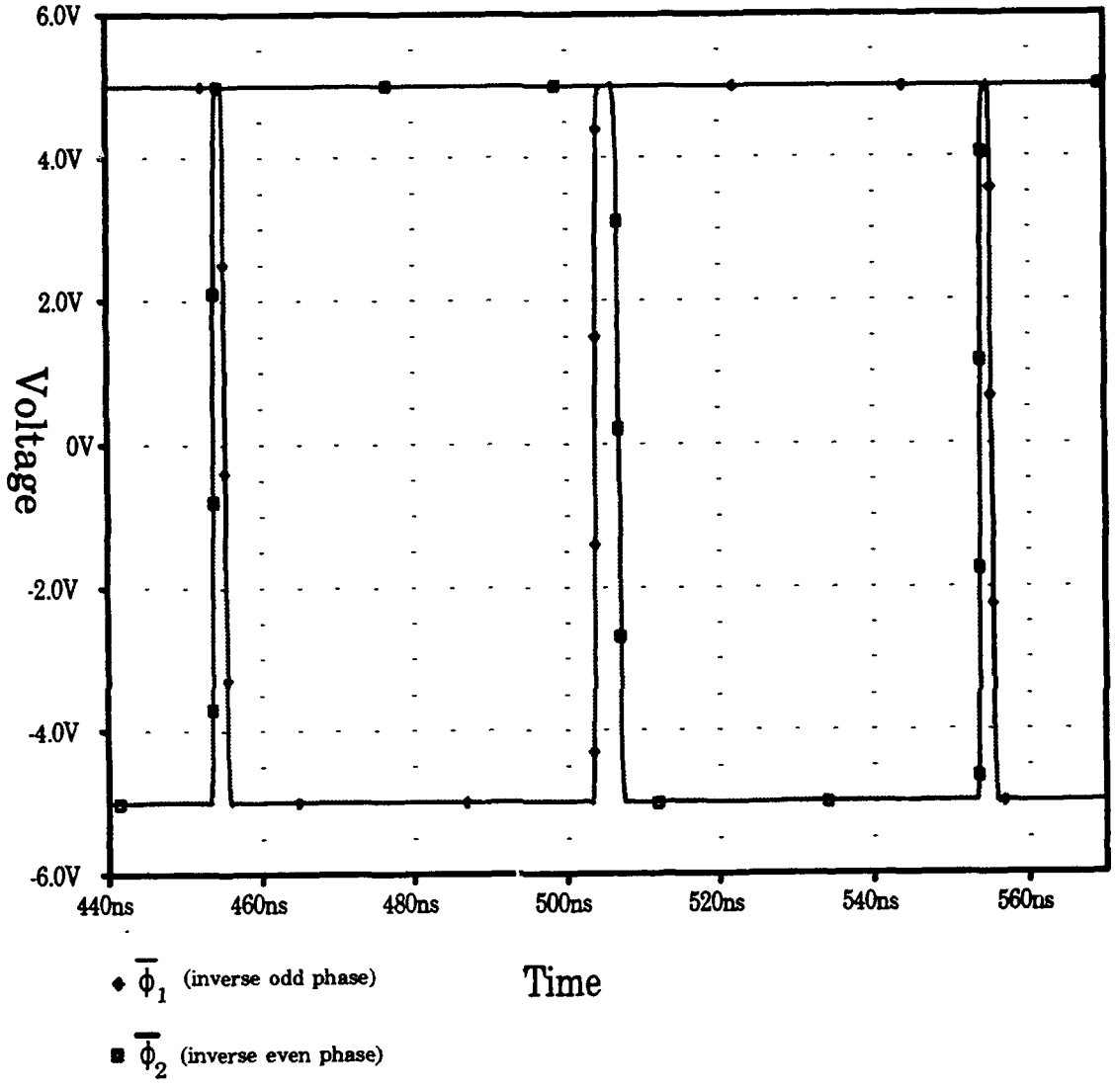
C. CLOCK CIRCUIT SIMULATION AND TESTING

Once the circuit was built the next step was to simulate the circuit to determine if the correct output was being produced and to determine if the final stage would be able to drive the required number of transmission gates. Figure 6.4 and Figure 6.5 show the results of testing the circuit to determine that the correct clock signals were produced. The resulting waveforms indicate the circuit performed as required. The next step was to ensure the circuit would be able to drive the required number of transmission gates.



Note: The plot is for a single-phase clock signal of 10MHz

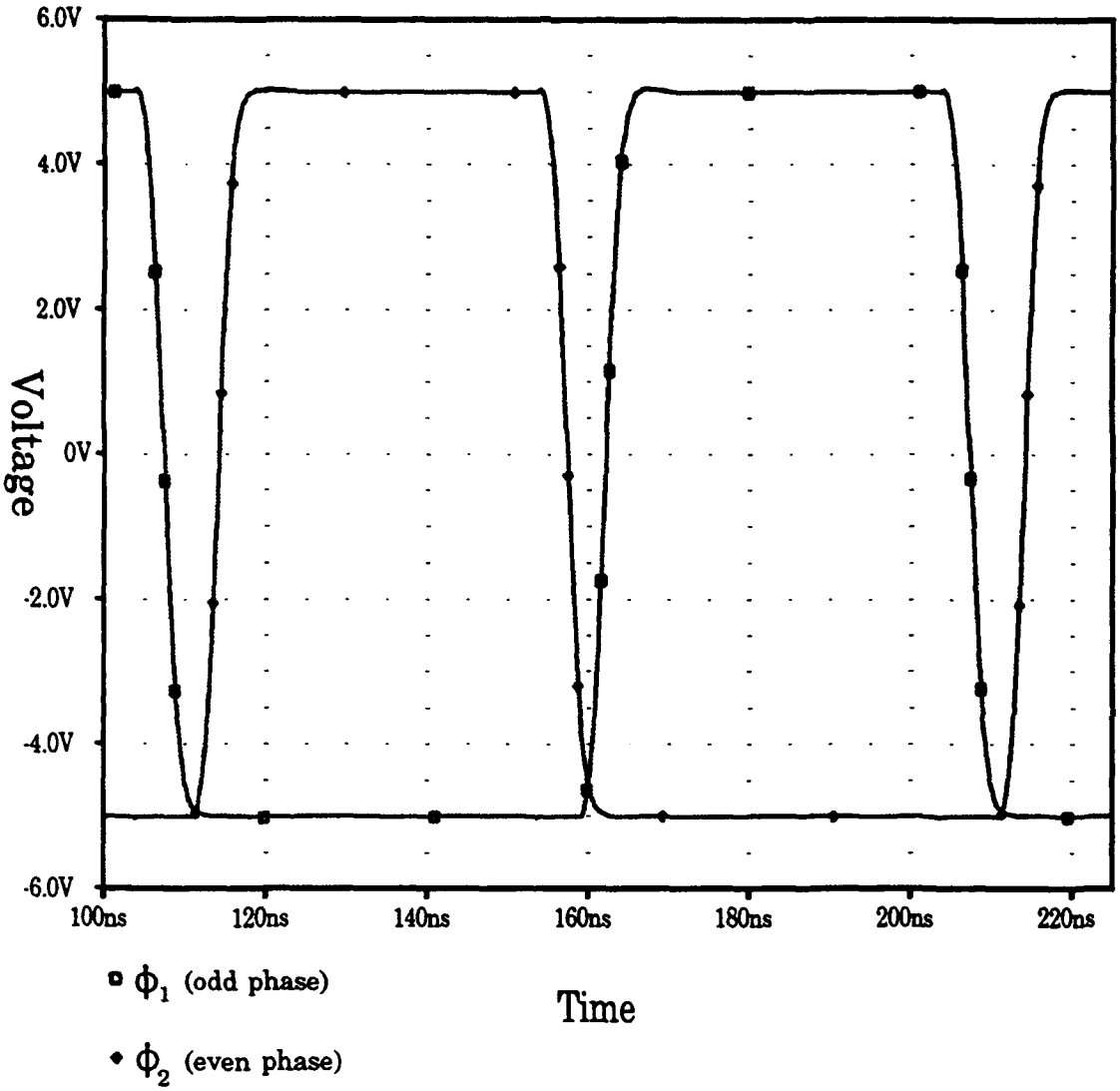
Figure 6.4 Clock Phases P1 And P2 (Odd and Even)



Note: The plot is for a single-phase clock signal of 10MHz

Figure 6.5 Clock Phases NP1 And NP2 (Inverse Odd And Inverse Even)

To test the circuit under load, the PSPICE test file was modified so that each phase of the clock was driving eight transmission gates. Figure 6.6 illustrates the performance of the circuit while under a load. The switching speed requirements for this circuit dictate that the design be able to handle single phase clocking rates of about 1MHz. This circuit as simulated can easily handle a master clock rate of 10MHz.



Note: The plot is for a single-phase clock signal of 10MHz.

Figure 6.6 Clock Phases With A 32 Transmission Gate Load

Additional information gained from this simulation was an estimate of the amount of current the circuit would draw. In CMOS circuits the amount of current used under static conditions is very small, usually in the microamp range but, during signal transitions in the circuit the amount of current usually reaches the milliamp range. The information about the current drawn under load is then used to determine the size of the metal power lines for the circuit. This information is important because if the power lines are made too small then there can be a problem with electromigration. Electromigration is a phenomena that results in an open circuit in the signal line and ultimately failure of the microchip. The plot in Figure 6.7 shows the amount of current required during the transition between phases in the clocking circuit. From these results, it is clear that the power lines need to be able to carry at least 9mA of current. A conservative estimate for how much current a metal line can carry is approximately 0.5mA to 1.0mA per micron of metal width [Ref. 11:pp 144]. Therefore, the power lines into each clocking circuit were designed to total more than 9μm in width.

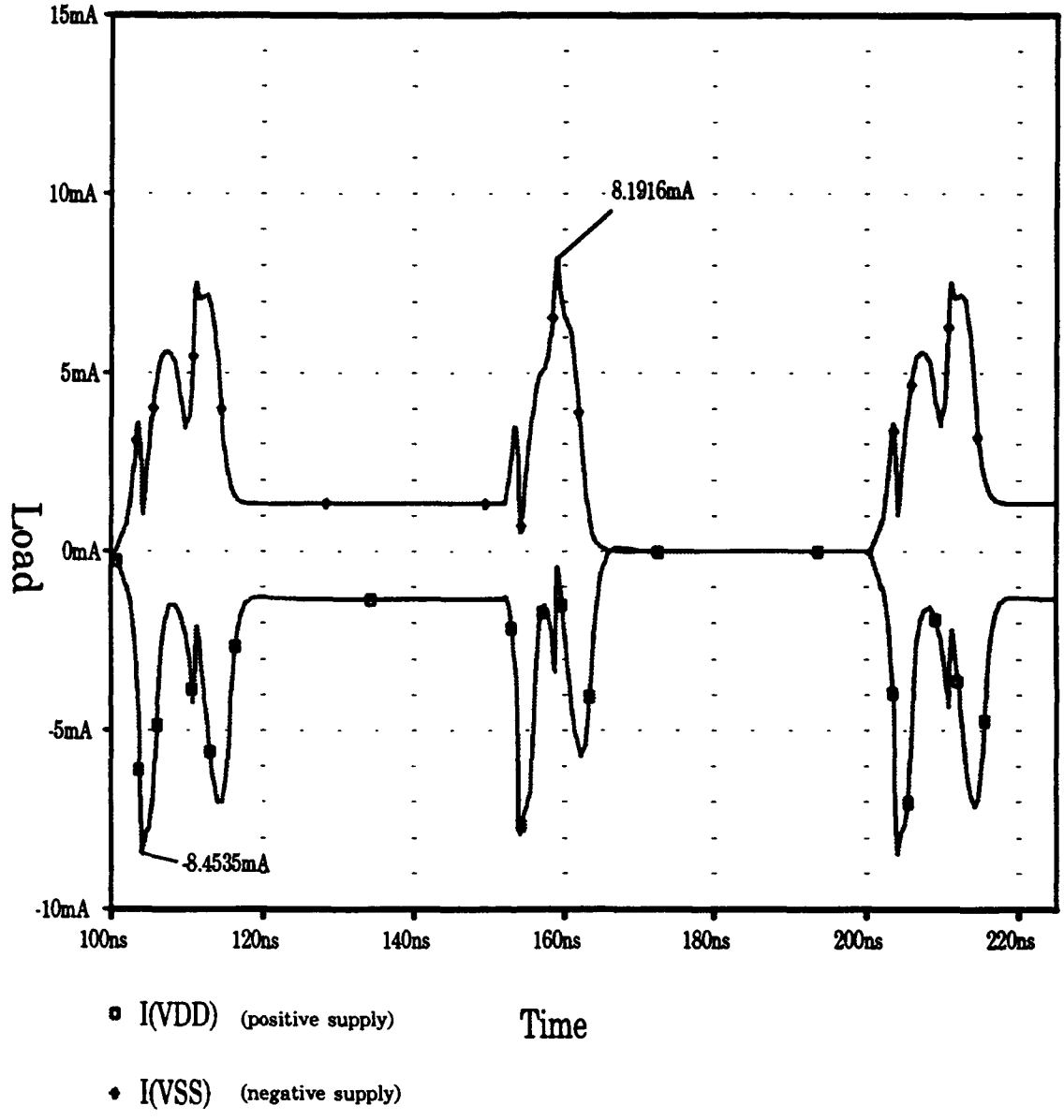


Figure 6.7 Clock Circuit Current Requirements Under 32 Transmission Gate Load

VII. THE COMPLETE CIRCUIT LAYOUT GEOMETRY

A. THE APPROACH TO THE OVERALL MICROCHIP DESIGN

This chapter deals with the design and methods used to complete the layout of the eight operational amplifiers, thirty-two transmission gates, two clocking circuits and the four groups of switched capacitors within the area available on the microchip. The basic approach was to divide the area into four separate subcircuits. These subcircuits corresponded to the four different stray insensitive composite operational amplifier topologies being implemented. Each subcircuit was then arranged in the available area according to some basic guidelines and with the requirement that each section match up with the other three sections when placed together in the completed design.

B. GUIDELINES FOR CIRCUIT LAYOUT GEOMETRY

One of the difficulties when using a fully custom microchip production process is the seemingly infinite number of ways the available area can be used to implement the desired circuit. This being the case, there was a need to limit the possible ways the circuit could be placed into the available area and at the same time avoid geometries that would create a less capable design with undesirable characteristics. As was stated above, this circuit had a logical division into the four separate CNOAs. This logical division of the design did not conflict with other layout guidelines that were followed. Reference 9 pp. 513 - 524 provided the guidance to optimizing the arrangement of the circuit. The

following paragraphs discuss the guidelines, their purpose and how the circuit was arranged to follow these design considerations.

One of the problems that can arise in a chip which contains both analog and digital components is that noise can be injected into the analog portion of the circuit from the power, ground and clock lines. The power lines supplying the digital portion of the circuit have large current spikes which correspond to the switching of the transistors in the network. If the same lines are used to power the analog portion of the design these current spikes would introduce noise into the analog power lines. This noise was eliminated in the chip design by providing complete separation of the analog power lines from the digital power lines. In addition, separate bonding pads leading to separate external pins were provided for both analog and digital power supplies. The clock lines can inject noise into the signal path through the gate to source and gate to drain capacitance. However, this effect was minimized in this design because the process uses a self aligned gate which results in a reduced gate to source and gate to drain capacitance. The ground used in the design was only connected to the analog portion of the circuit. Thus, the best way to keep noise from contaminating the system through the ground line was to ensure that this pin was connected to a noise free external ground.

Another design guideline was to use the analog power lines to bias the last four inverters of the clocking circuit. From Figure 6.1 it can be seen that the last four inverters provide the even and odd phases of the two phase non-overlapping clock signals and their inverses. Using the analog power lines for this portion of the design helps to reduce the digital noise in the clock signals.

In order to reduce the amount of noise coupled into the inverting input of the operational amplifier, it was important to minimize the noise in the lines connected to the inverting terminal. This was accomplished by ensuring the bottom plate of the parallel plate capacitor was never connected to the inverting input. The bottom plate of the parallel plate capacitor was constructed with metal 1 and the top plate was constructed with metal 2. The bottom plate is closest to the substrate and a parasitic capacitance is formed between the bottom plate of the capacitor and the substrate. This provides a path for coupling substrate noise into the amplifier and this noise is most pronounced if the bottom plate is connected to the inverting terminal of the amplifier. Also, to prevent noise from coupling into the OA, the input node lines and other signal lines were constructed to avoid crossing one another if at all possible. If this was not possible then the layout was done to minimize the amount of overlap when signal lines and input lines had to cross each other. An additional technique used when organizing the layout of a chip, is to place identical components in the same physical area of the chip. Figure 7.1 is a diagram of the circuit layout which shows how the components were organized into separate areas on the chip.

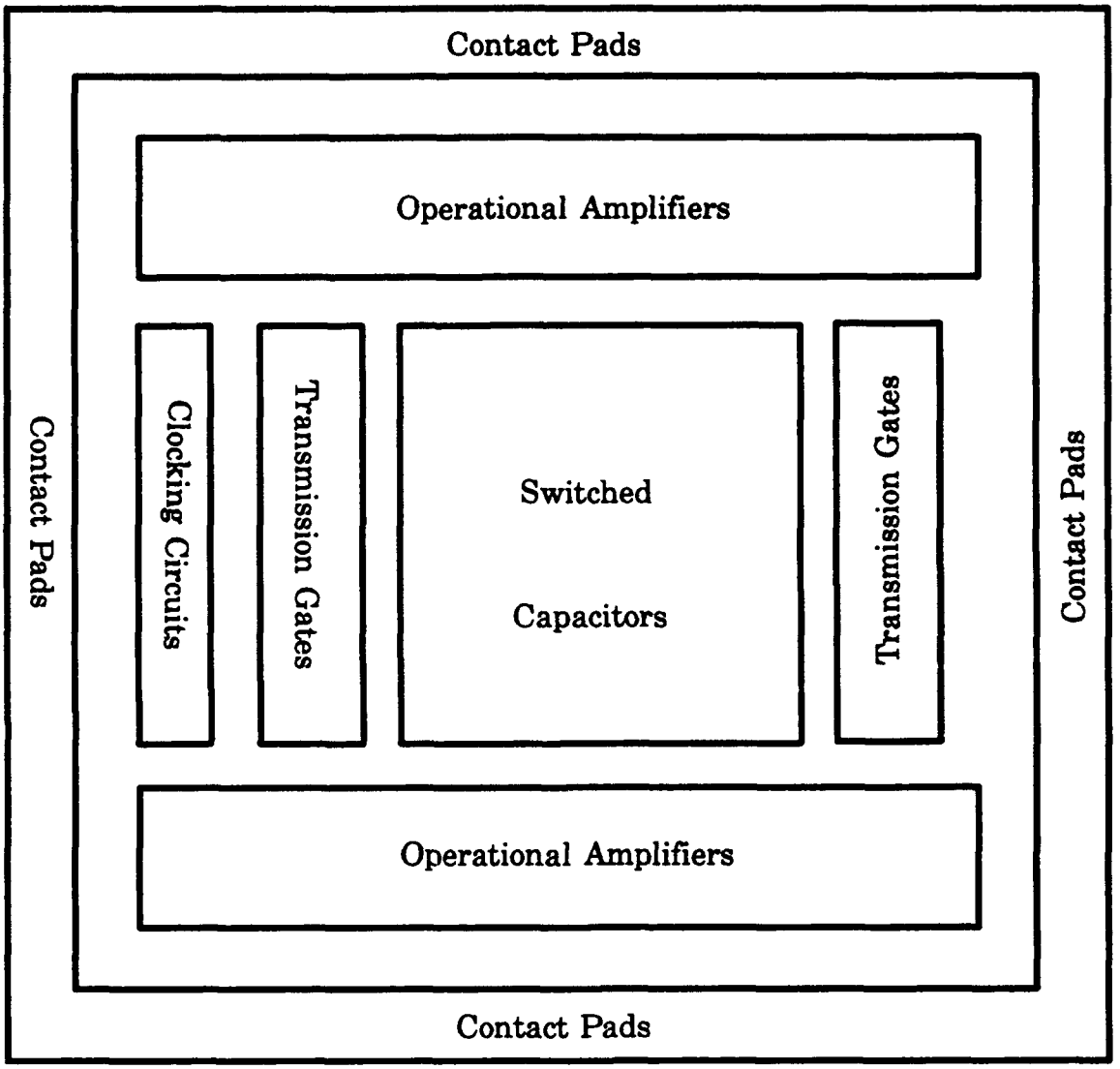
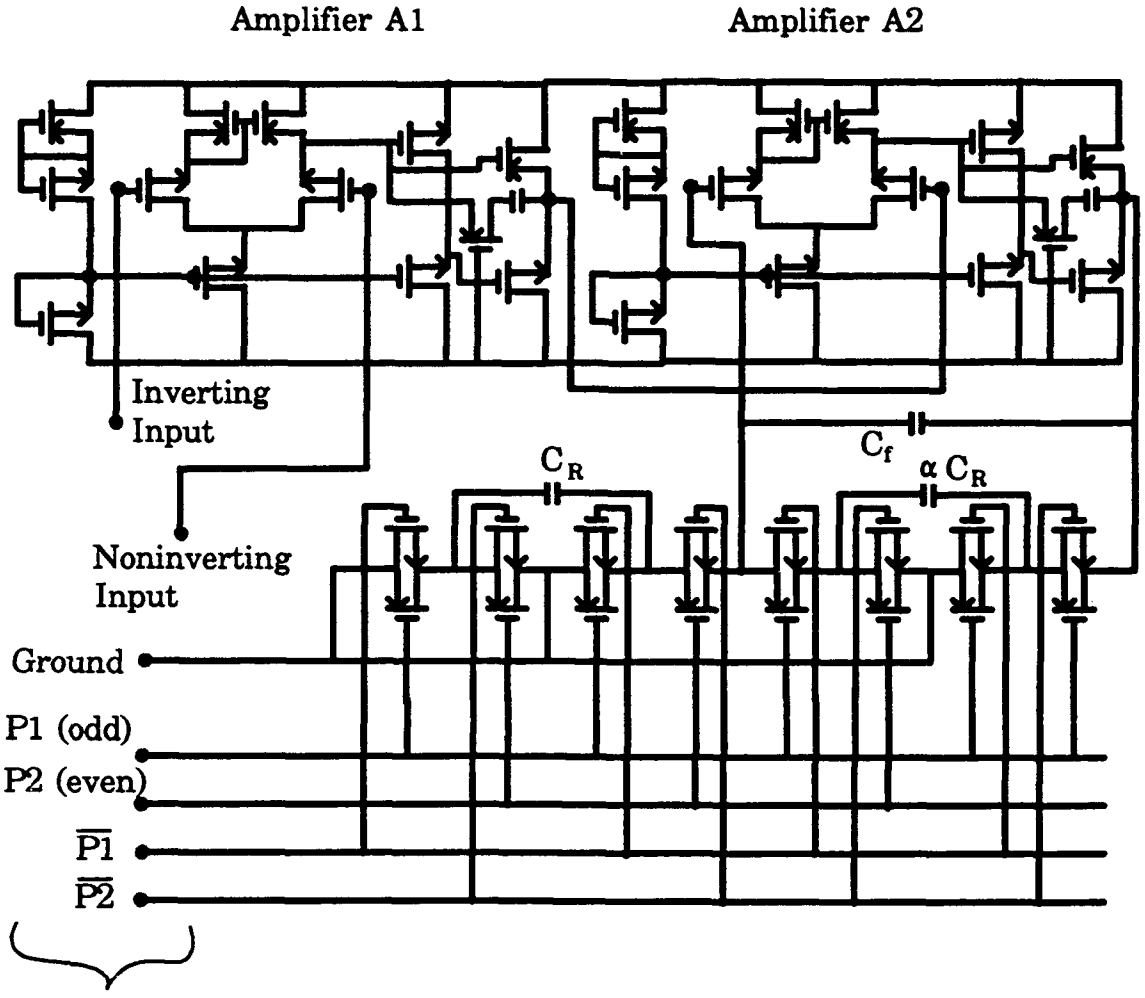


Figure 7.1 General Microchip Layout Organization

C. CNOA AND ENTIRE CIRCUIT LAYOUT ORGANIZATION

The circuit layout guidelines described above were followed when determining the layout geometry of the individual CNOA networks. The four different topologies described in Chapter II were constructed one at a time. Then the four layouts were incorporated into a single design to which the contact pad circuitry and connecting metal lines were added.

The circuit diagram presented in Figure 7.2 is a transistor level network that represents the CNOA, TSC_C2OA-2, implementation. This diagram does not include the transistor level two phase non-overlapping clock circuit, but it does indicate where the two phases and their inverses connect into this network. See Figure 6.2 for a transistor level circuit diagram of the clock. The TSC_C2OA-2 will be used to illustrate the implementation of the CNOAs. The other three CNOAs where implemented in a similar manner.



Signal lines from the two phase non-overlapping clock circuit

Figure 7.2 TSC_C2OA-2 Transistor Level Circuit Diagram

Figure 7.3 shows the layout geometry of TSC_C2OA-2. This figure indicates where all of the major components are in the circuit and it shows how the interconnections of these components was accomplished. This basic geometry was used as the basis for all four of the CNOA layout geometries.

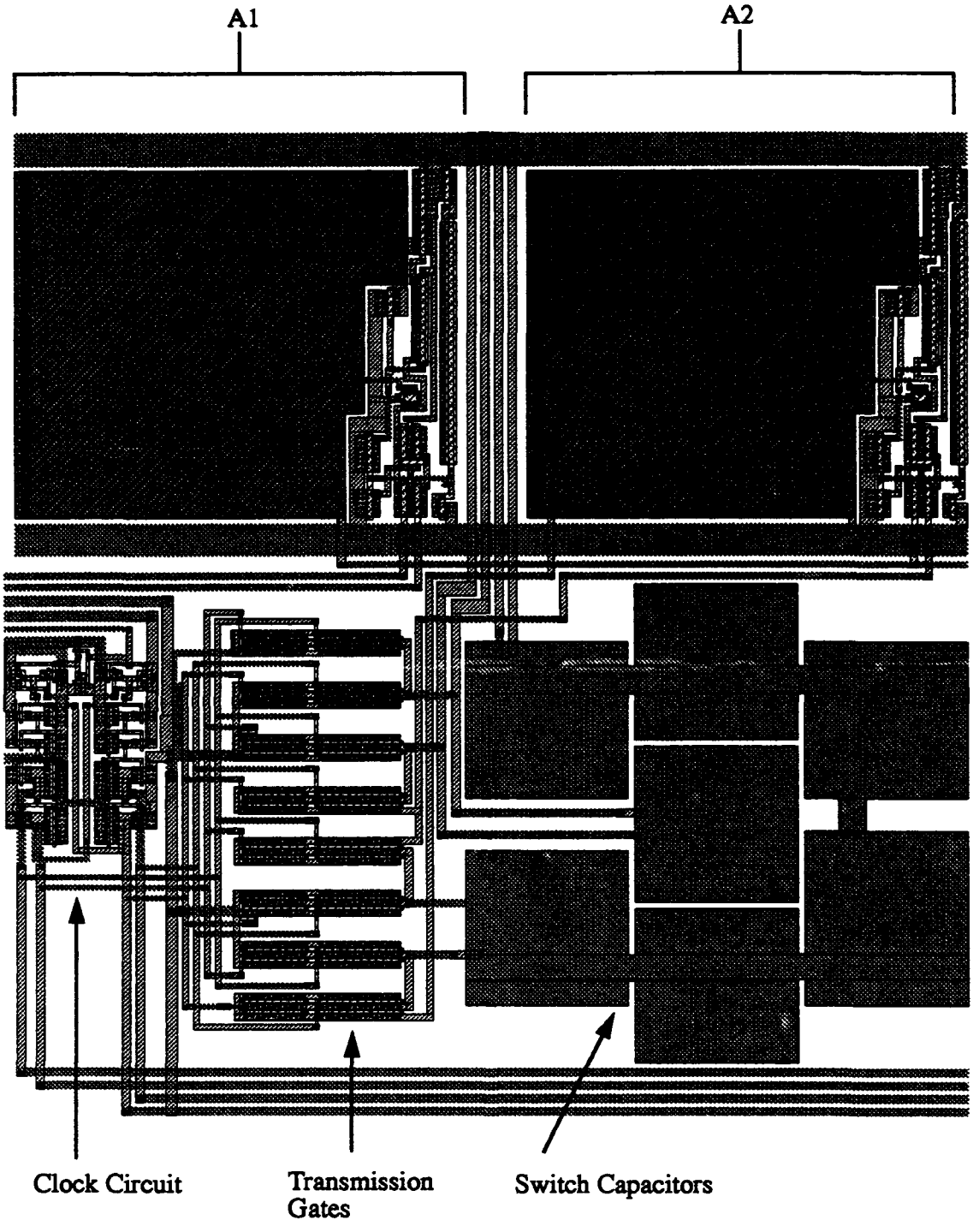


Figure 7.3 TSC_C2OA-2 Layout Geometry

Figure 7.4 shows the layout geometry of the entire microchip, including all four CNOAs, the clocking circuits, the amplifiers, the capacitors and the bond pads that make up the pad ring, refer to Figure 7.1 for a general chip layout. Figure 7.4, also illustrates the final design that was submitted for fabrication. The following is a list of labels including a short description of their functions:

1. Analog Vdd - bond pad to the positive power for the analog circuit.
2. Analog Vss - bond pad to the egative power for the analog circuit.
3. Digital Vdd/Vss - bond pads for positive/negative power for the digital circuit.
4. Cr1x, Cr2x, aCr1x, aCr2x - provide access to place capacitance in parallel with the on chip capacitors. If x = 1 it connects to TSC_C2OA-1, x = 2 connects to mOFR_C2OA-1, x = 3 connects to TSC_C2OA-2, and x = 4 connects to mOFR_C2OA-2.
5. -Vx - is the inverting input to the CNOA, x functions as described above.
6. +Vx - is the non-inverting input to the CNOA, x functions as described above.
7. Outx - is the output of the CNOA, x functions as described above.
8. TPx - provide access to an internal node, x functions as described above.
9. CLK - is the bond pad that supplies the external Master Clock input.
10. GND - is the bond pad that connects to an external ground.

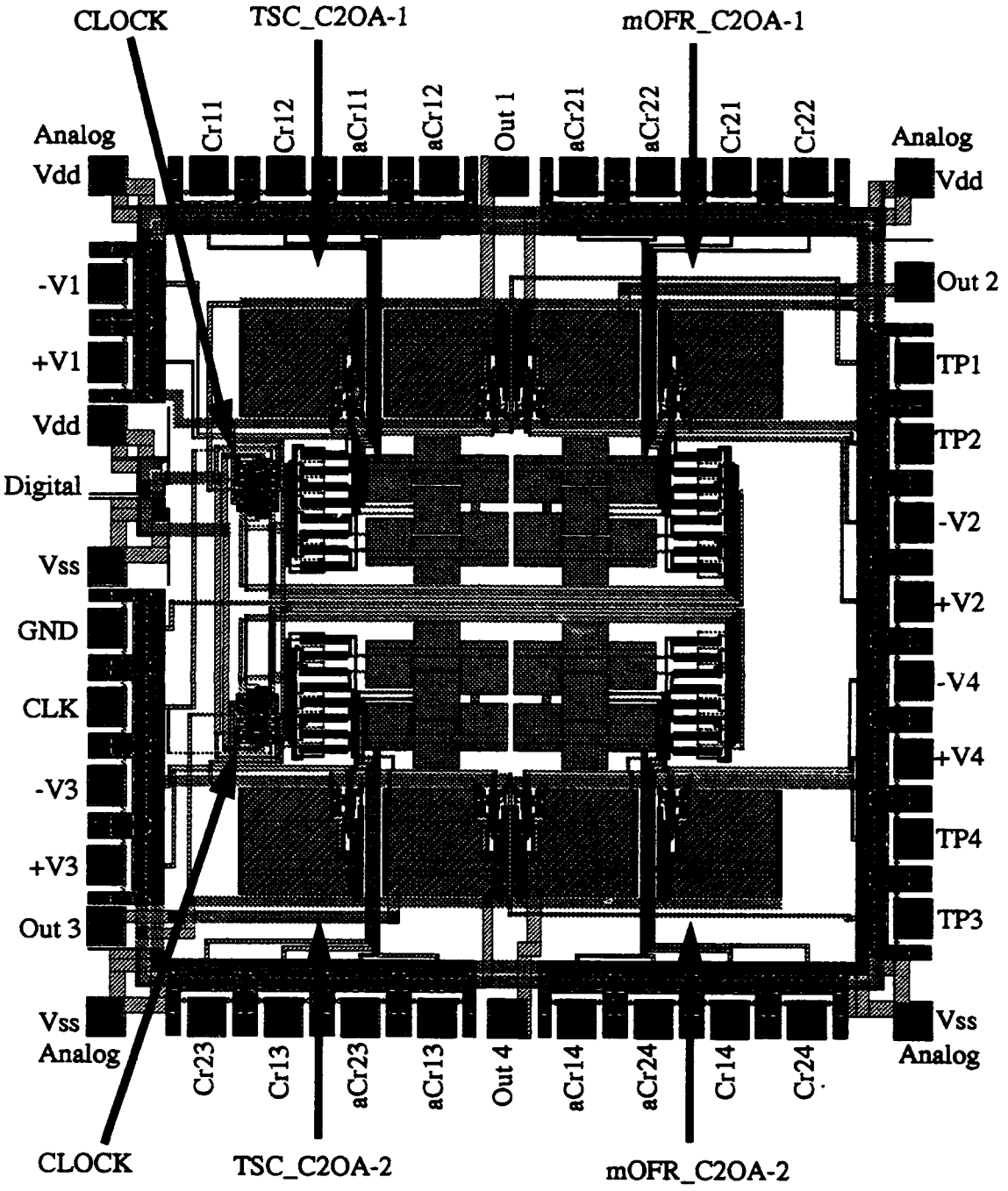


Figure 7.4 Complete Microchip Layout Geometry As Submitted For Fabrication

D. SIMULATION AND TESTING RESULTS

The microchip was manufactured and received back from the foundry after approximately eight weeks. Four, forty pin, dual in line packages were received. The initial step taken in testing was to connect the positive power supply, the negative power supply and the ground line. Next the power supplies were gradually increased in 0.25 Volt steps until the power supplies reached the + 5 Volt and -5 Volt design levels. During this initial power up stage the amount of current drawn was constantly monitored for any indications of latchup. The primary indicators of latchup are a sudden large surge in current, an extremely hot package, smoke emanating from the package or a combination of all of these indication. This initial power up of the chip did not indicate any latchup problems or Vdd to Vss shorts or power to ground shorts.

The next stage of the testing was to connect the CNOAs in a finite gain negative feedback configuration, add the master clock signal and the input signal. This configuration resulted in improper circuit performance and latchup. The latchup was indicated when the power supplies current increased to its maximum limit. Fortunately, the amount of current was not sufficient to cause chip destruction. After several attempts to connect the circuit, a configuration was discovered that allowed for circuit operation without causing latchup. Unfortunately, the first chip was destroyed will trying to come up with a configuration that would allow for operation of the circuit without latchup.

To prevent chip destruction, the power supplies were set to limit its maximum current to 100 mA. This was determined to be a safe level of current that would not

result in chip destruction if latchup occurred. At the first sign of latchup the power supplies were turned off and the clock and input signal were also turned off. Initially, the circuit was very sensitive to changes in the master clock input. Rapid changes to the clock almost always caused the chip to latchup. Therefore, the clock frequency was changed with the clock disconnected from the circuit. After gaining some experience working with the circuit the latchup problem became manageable.

The next step was to set up the CNOAs in finite gain negative feedback configuration to investigate the gain bandwidth product of the circuit. After some trial and error a unity gain negative feedback configuration was selected to allow for a relatively large input signal without causing the output to be limited by the power supplies. The initial results indicated that the output had a significant amount of noise which occurred at the same frequency as the clock. In an attempt to filter out the high frequency noise caused by the clock a 2.2 nF capacitor was placed on the output. This was effective in attenuating the clock noise but it also had the undesirable effect of limiting the bandwidth of the amplifiers. This resulted in an inability to determine the actual gain bandwidth product of the circuit. To confirm that this was the correct interpretation of the observed results a PSPICE simulation was performed on a single amplifier with a 2.2 nF capacitor on the output. The results of this simulation are shown in Figure 7.5.

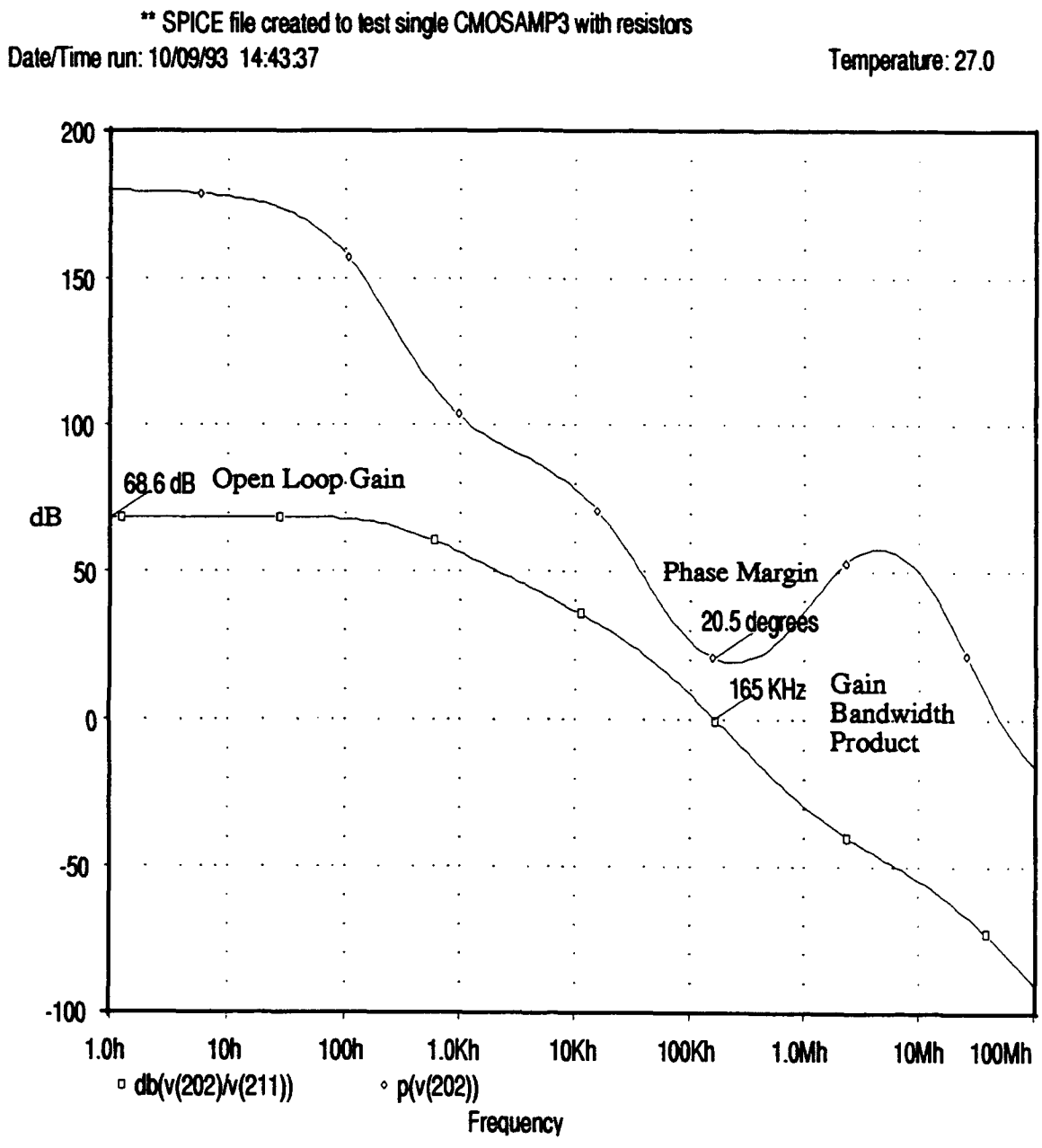
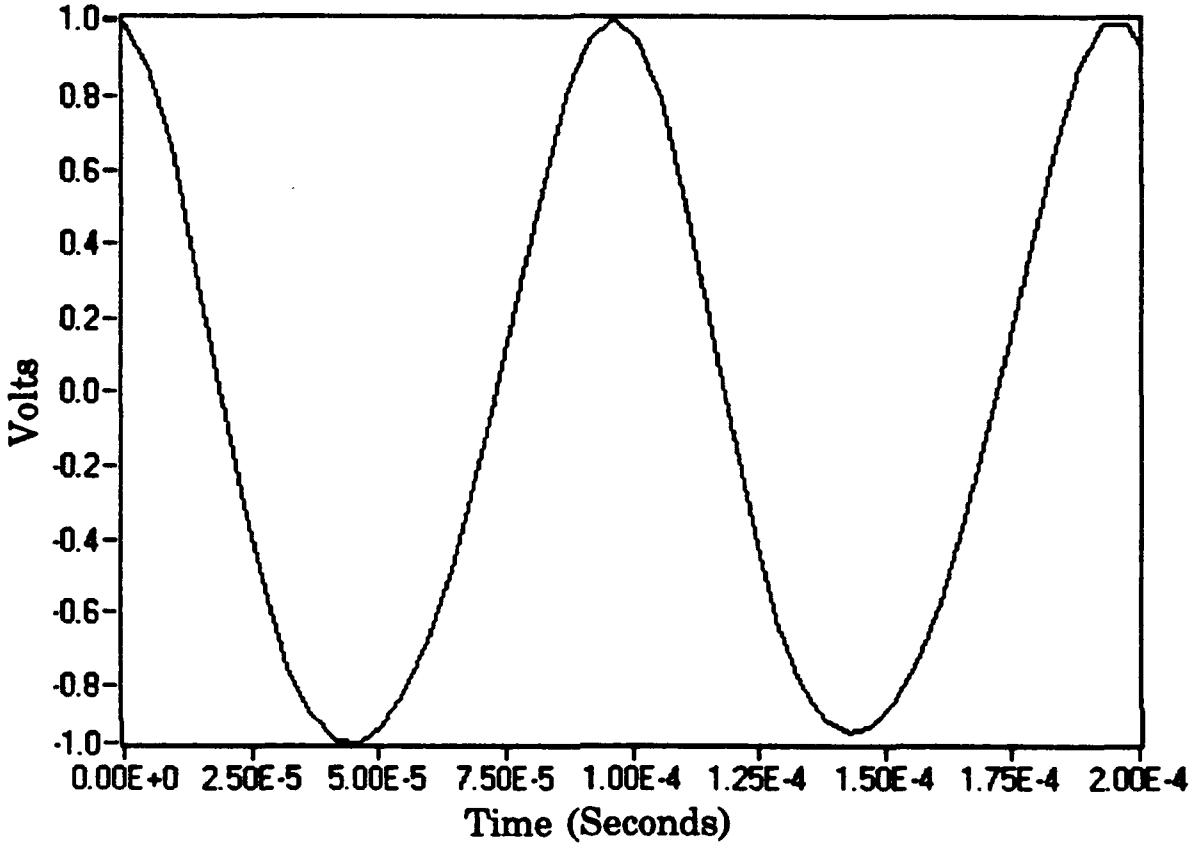


Figure 7.5 CMOS Amplifier Frequency Response With A 2.2 nF Capacitive Load

There are several important aspects to note concerning this simulation. First, the simulation was performed with the SPICE parameters that were determined and provided by the manufacturer for this particular fabrication run. Second, the simulations performed previously were done with less complete and less up to date simulation parameters. Third, the simulation gain bandwidth product of 165 KHz was very close to the 130 KHz that was observed in the laboratory testing. It is also important to note that there was very little variation among the three remaining chips with respect to their gain bandwidth products.

Figure 7.6 illustrates the observed output from laboratory testing of TSC_C2OA-2. The input was a 0.1 Volt peak sine wave at 10 kHz and the circuit was placed in a negative feedback, finite gain of 10 Volts/Volt. This result is representative of the data obtained for all of the chips and the CNOAs tested. The results illustrated in Figure 7.7 are from a PSPICE simulation that was set up to resemble as close as possible the actual test circuit in the laboratory. The SPICE parameters used were those supplied from the manufacturer. The simulation results are almost identical to those observed in the laboratory.



Note: Input was a 0.1V sin @ 10KHz, the output is shown on the graph above. The output plot was produced by using a data acquisition system. This resulted in a filtering effect on the data so that the 10MHz clock noise that was observed in the laboratory is not represented in this plot.

Figure 7.6 Laboratory Test Results

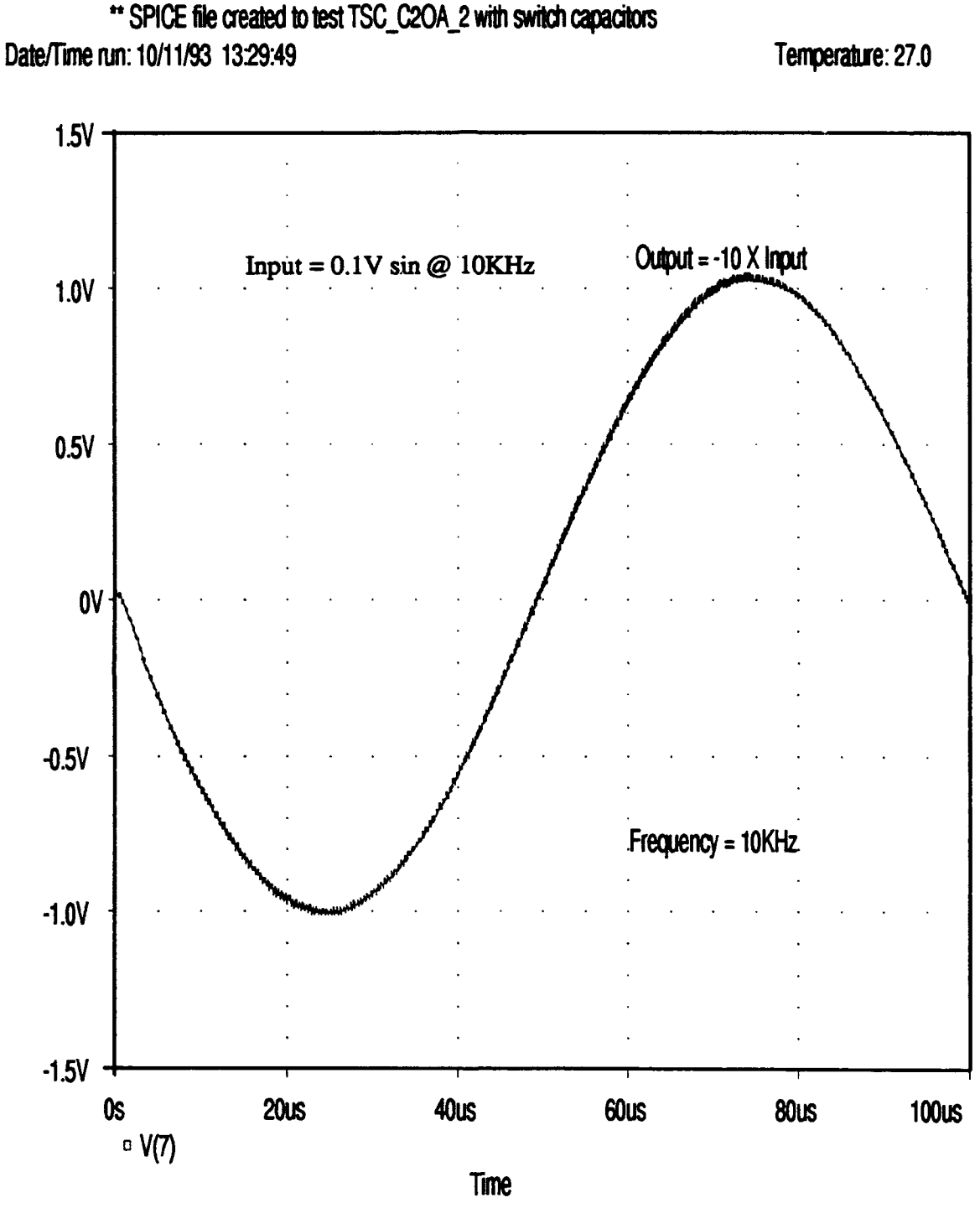


Figure 7.7 PSPICE Simulation Results Of Laboratory Circuit

E. ANALYSIS AND CONCLUSIONS

The results of the testing indicate that the overall circuit performance was significantly worse than was indicated by the prefabrication simulations. The primary cause of this deficiency in performance was due to the digital noise that was feeding into the analog portion of the circuit. To remove the clock feed through noise a low pass filter was connected to the output. This resulted in a cleaner output, but it also prevented accurate determination of the gain bandwidth product and the slew rate of the CNOAs. There are several reasons for the less than expected performance of the circuit. The following is a discussion of the most likely causes of this limited performance.

The most significant problem with this chip was the extreme digital noise that was feeding into the analog signal path. This was caused by several factors. First, there was not enough attention given to isolating the digital noise. Additional design modifications such as grounded (analog ground) guard rings surrounding the amplifier differential pairs would have helped to isolate this high gain input from the digital noise in the substrate. Second, the desire to reduce the on channel resistance of the transmission gates resulted in a substantial increase in the gate to drain and gate to source capacitance. These capacitances provided a means for coupling the digital clock signals into the analog signal path. This could have been prevented by using minimum sized transmission gates. The amount of the added impedance would not be large enough to affect the accuracy of the ratio of the capacitors. Third, more simulations should have been done using more up to date simulation parameters. The desire to meet a fabrication deadline resulted in

accepting simulations that were not as thorough as would have been desired. Fourth, the process being used was optimized for digital circuits. Therefore, the noise reduction is not as critical because digital circuits are usually designed with large noise margins and can operate with a level of noise that would be extremely detrimental to the performance of an analog circuit. This process also created some inconsistencies in the stated purpose of using switched capacitors to replace resistors in VLSI technology. One reason for using switched capacitors was to reduce the area that would be required to produce a comparable resistor. This process did not provide any layers that could be used to create accurate, large capacitors. The result was that the capacitors required most of the layout area and their accuracy was poor. This could only be corrected by using a fabrication process optimized for analog circuits. Finally, the use of two clock circuits created twice as much noise as one clock circuit. The need for two clock circuits resulted from the need to drive large transmission gates so the use of minimum sized transistors would eliminate this requirement.

Another consideration, not directly related to improving chip performance, that should have been considered was the learning curve involved with an initial design. It would have been more prudent to reduce the number of CNOAs placed on the chip and in return provide access to more of the internal nodes. This would have allowed for more indepth testing and better analysis of any short falls in performance. Additionally, the unused area would have provided room to place a single amplifier on chip that could have been tested independent of the switched capacitor circuit. This would have allowed for analysis and evaluation of the operational amplifier itself, to determine if the design

should be modified. This was the first analog VLSI chip to be manufactured at the Naval Postgraduate School using this process. The experience gained from this chip fabrication was used to design and produce a second chip. The follow on design will be discussed in the next chapter.

VIII. THE LOW NOISE ANALOG CMOS PROCESS

A. CHARACTERISTICS AND ADVANTAGES OF THE ANALOG PROCESS

One of the reasons the first microchip did not perform as well as desired was due to the fact that the process used for fabrication was optimized for digital circuits. Although this design incorporated both digital and analog elements, the performance of the analog circuits were more crucial to the overall performance of the CNOA. Therefore, a process optimized for analog applications is preferable to a digital process. Also, it is important to note that the performance requirements for the digital portion of the network is not as stringent as the performance limits of the digital CMOS process. Thus, the reduction in performance of the digital circuit built in an analog process will not affect the overall performance of the network. The low noise analog process was not chosen for the fabrication of the first microchip because, the process was unavailable at that time.

Another important advantage of the analog process was the capability to build accurate capacitors (10%) and use smaller layout for the same size capacitor built in the digital fabrication process. This was made possible by access to an additional polysilicon layer called polysilicon two or electrode. This layer was not available in the digital process. Although it can be used to produce transistors, the primary purpose of the second layer of polysilicon was to provide an efficient means to build parallel plate capacitors. In fact, the plate to plate capacitance of the polysilicon layers provides an order of magnitude increase over the metal to metal capacitance available in the digital

process. This resulted in much smaller layout area for the capacitors, as well as, much more accurate capacitance values.

Another significant advantage of the analog process is the emphasis on noise reduction in optimizing the fabrication process. The most significant problem with the first microchip was the extreme amount of noise that contaminated the signal path. Design changes that will be discussed later can prevent some of the noise injection but, it is also important to have a fabrication process designed to keep noise out of the signal path.

B. REDESIGN OF THE CNOA FOR THE NEW PROCESS

It was necessary to redesign all of the components of the first microchip except for the two phase non-overlapping clock circuit. There were several reasons that made the redesign imperative. The primary reason was due to the new process. In order to take advantage of the new capabilities offered by the process, the amplifier had to be modified. The basic circuit for the amplifier remained the same. The significant reduction in the size of the compensation capacitor made it possible to increase the size of the transistors in the amplifier. Increasing the size of the transistors improved the open loop gain as well as the load capability of the amplifier. Another change to the amplifiers was the addition of guard rings around the differential, high gain, input transistors as well as the transistors acting as current sources for the gain stages. The guard ring is a diffusion layer that is heavily doped with the same type of dopant as the substrate. This results in a good conductive connection to the substrate. The guard ring is then connected to signal

ground and functions to draw away stray currents from the substrate that could inject noise into the circuit. Figure 8.1 shows the layout of the redesigned amplifier. Figure 8.2 is a PSPICE plot of the open loop frequency response. For a circuit diagram of the amplifier refer to Figure 4.1.

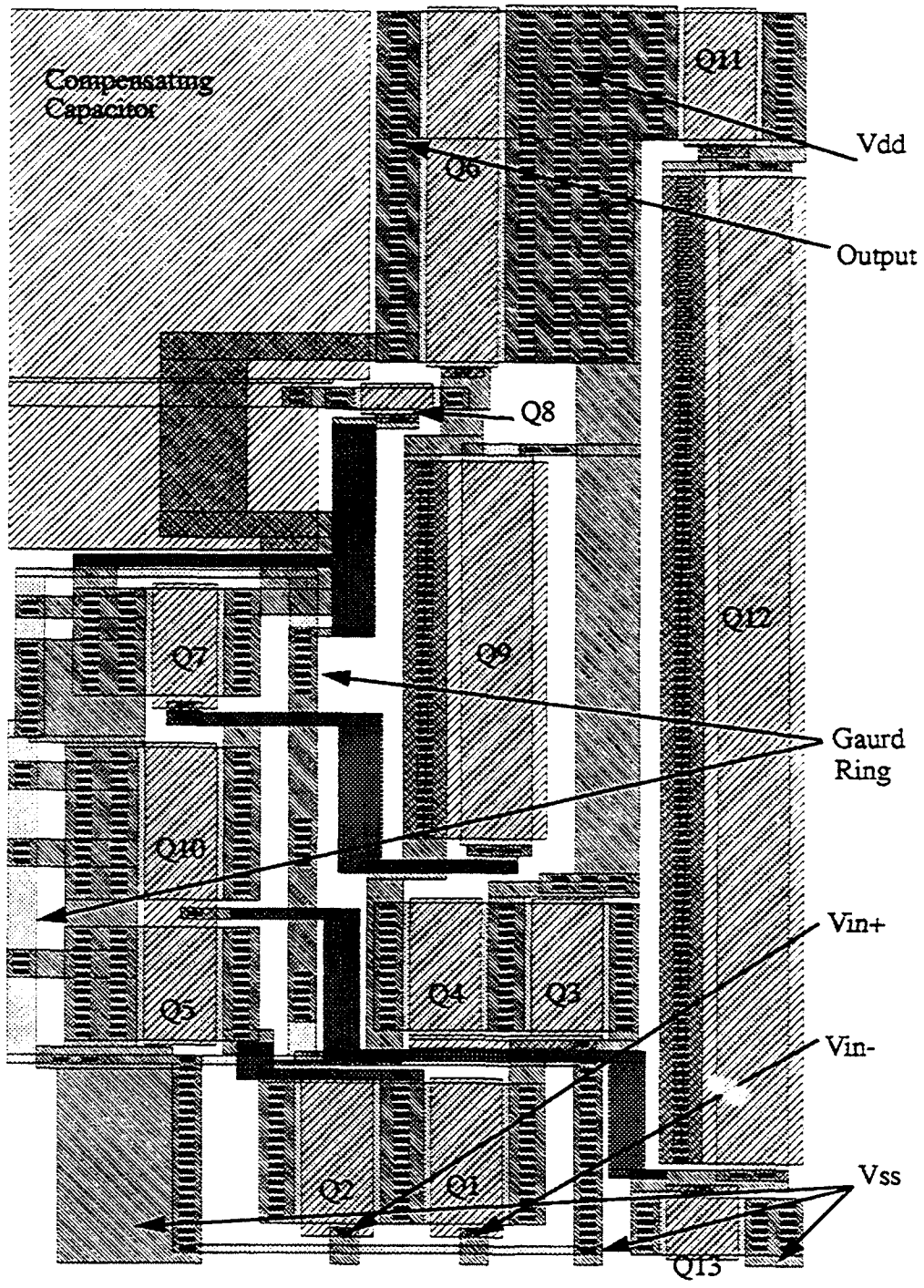


Figure 8.1 Layout Geometry Of The Redesigned Amplifier

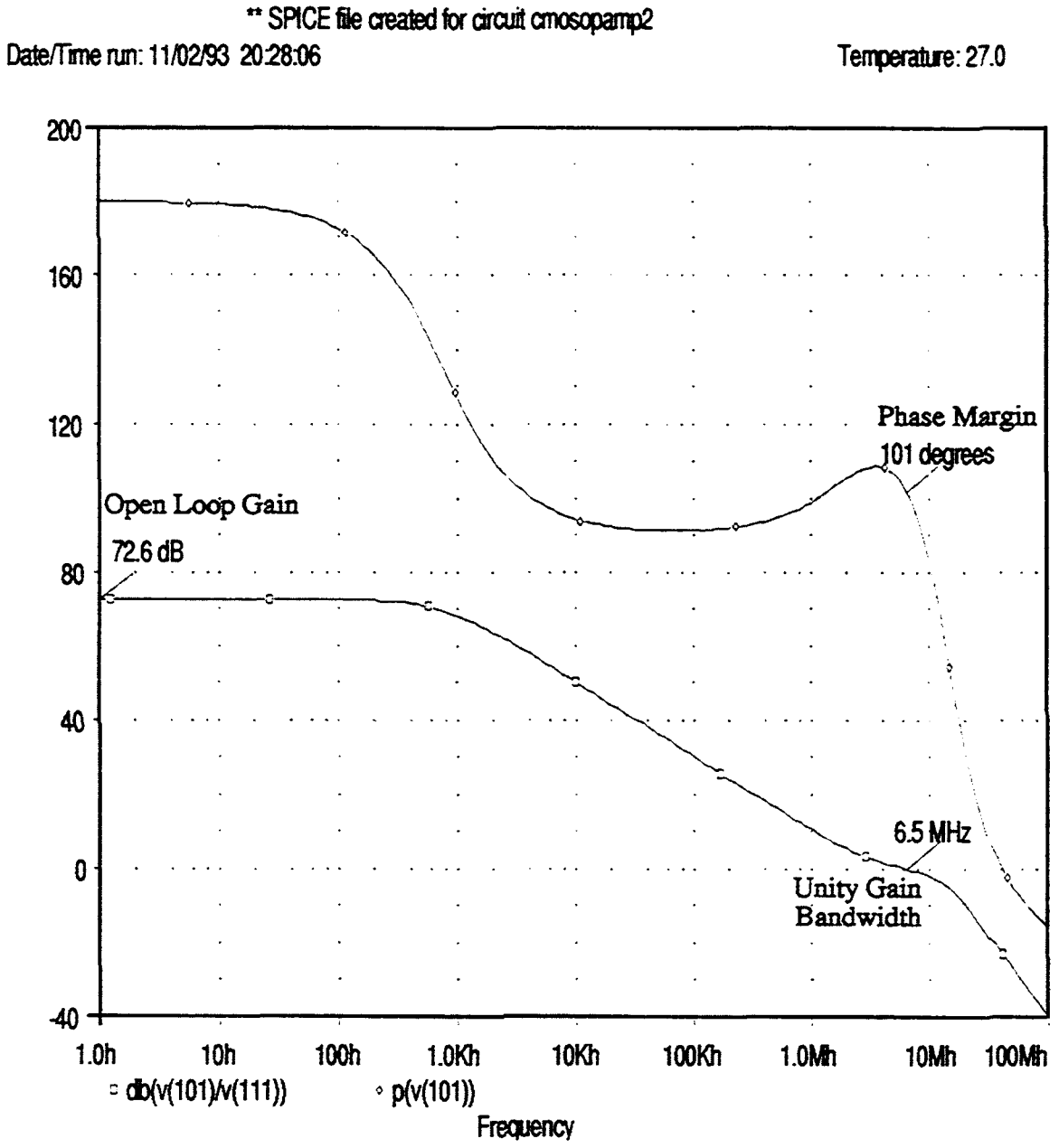


Figure 8.2 Open Loop Frequency Response Of The Amplifier

Another noise reduction technique in the new design was the use of a minimum sized transmission gate to replace the much larger transmission gate of the original design. This results in minimization of the gate to drain capacitance and the gate to source capacitance. Reduction of these capacitances is important to eliminate or at least significantly reduce the clock feed through problem experienced in the first microchip. Clock feed through was probably the largest contributor to the noise in the signal path on the previous design as mentioned before.

A major change in the second design was a decision to use a more conservative overall layout. The CNOAs that performed the best in the first design were the TSC_C2OA-2 and the mOFR_C2OA-2. These were the only two designs implemented on the new chip. Also, separate isolated single amplifiers were placed on the chip and access was provided to their inputs and outputs for testing purposes. In addition to this, all four phases of the clock were connected to output pins so they could be observed and access was provided to all of the significant nodes on the CNOAs.

Finally, one additional feature was added to the design. This new feature provides for programming α, the ratio between the two switched capacitors. The implementation uses 4 digital lines that allow for selection of 16 different ratios, from 1 to 16, using a simple binary coding scheme. The programming could be done manually or by using microprocessor controlled signals or some other automatic control device. The addition of the programmable capability required very little additional chip area due to the improved capacitors design. Figure 8.3 shows the layout geometry of the new microchip illustrating the applications implemented. Figure 8.4 illustrates the programmable portion

of the microchip and its functionality. The following is a list of labels including a short description of their functions:

1. Pads Analog Vdd and Vss - pads that supply power all the bond pads.
2. Analog Vdd and Vss - provide power to the analog portion of the circuit.
3. Sxx - are the eight programming pads, each CNOA requiring four.
4. OUTx - are the output pads for the CNOAs and the single OAs.
5. -Vx and +Vx - are the inverting and non-inverting inputs to the CNOAs and OAs.
6. P1, P2 and the Inverses - are output pads for the two phase clock.
7. Digital Vdd and Vss - provide power to the digital portion of the circuit.
8. CLK - master clock input used to drive the two phase clocking circuit.
9. Vxx - internal test point for the CNOAs.

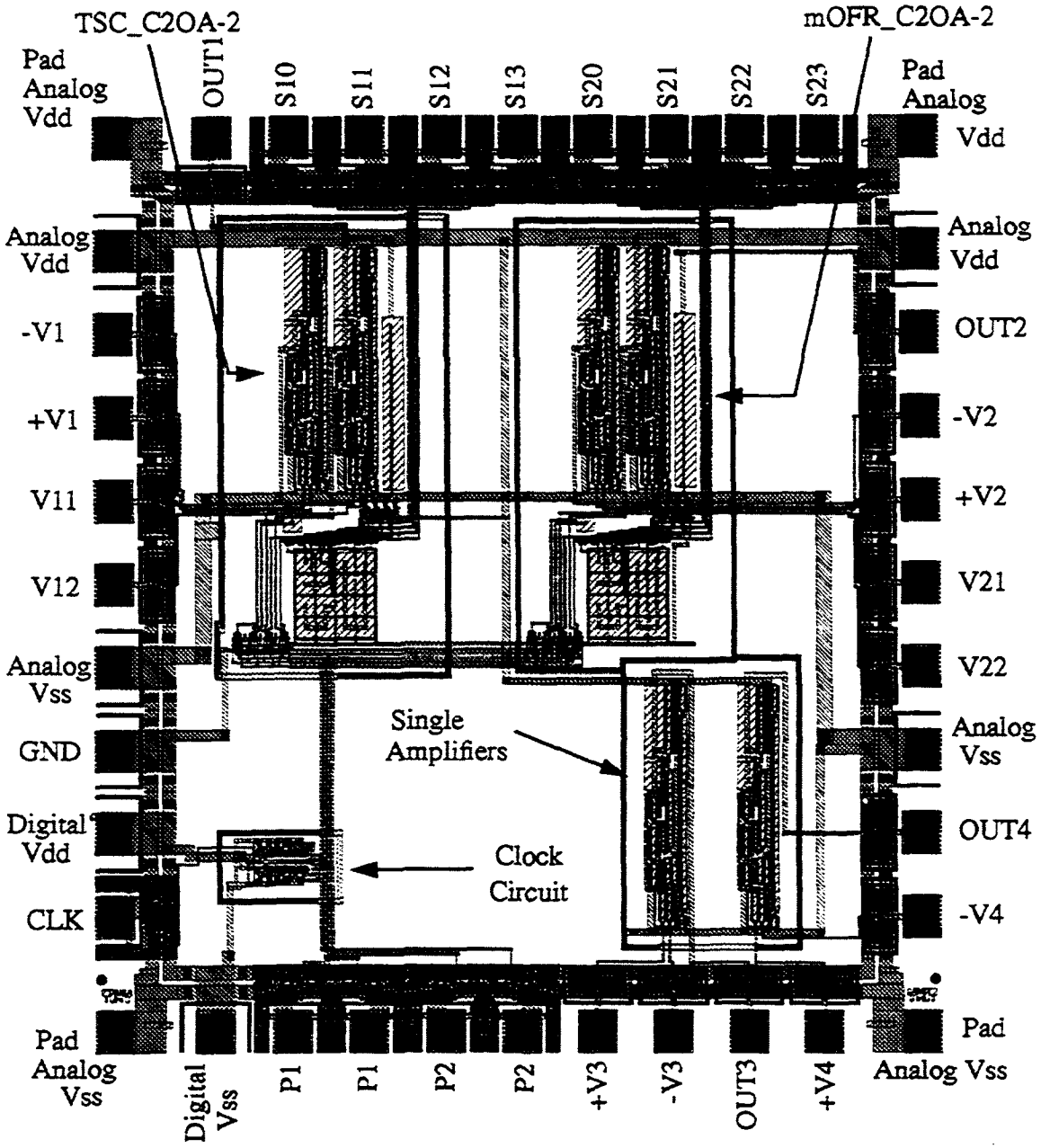


Figure 8.3 The Low Noise Analog Microchip Layout Geometry

Binary Truth Table

Binary Coding For Programming α				
S_3	S_2	S_1	S_0	alpha value
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

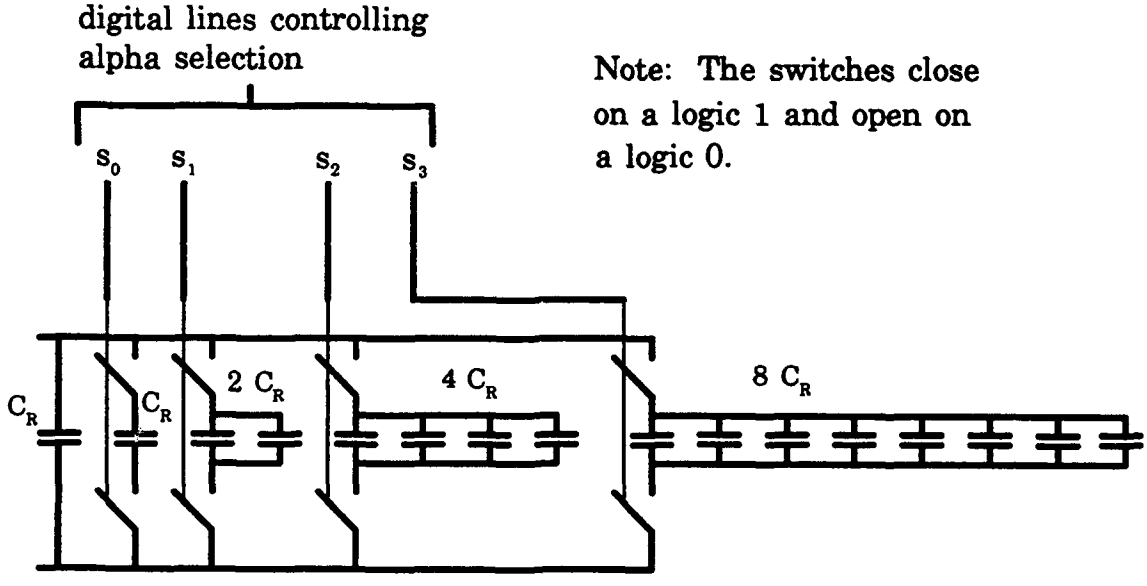


Figure 8.4 Truth Table And Circuit Diagram Of The Programmable Capacitor Ratio α

C. SIMULATION AND TEST RESULTS

One of the important areas that needed to be emphasized in the new design was simulation. Based on the experiences of the first design, it was clear more reliable and more accurate predictions of the overall circuit performance were needed. Using the laboratory observed results as a benchmark, several simulation formats were evaluated to determine which simulation produced results that most closely resembled the observed results. It is important to note that these simulation formats did not alter the structure of the circuits. The changes in the simulation were in the format of the simulation program and in the parameters used to define the NMOS and PMOS transistors.

As was mentioned in Chapter VII, the simulations for the original design were done with SPICE parameters which were not up to date and which did not include all of the process parameter specifications. Therefore, some of the parameters used were default values. When the first design was received back from the manufacturer, the documentation that accompanied the chip included the SPICE parameters developed from the fabrication run. These parameters were more up to date and much more complete than the parameters available for the original simulation. Having the actual fabrication parameters resulted in insignificant changes to the digital circuit performance but, the effect on the analog simulation was very significant. Fortunately, the new analog process provided SPICE fabrication parameters from a process run as of July 1993.

Another significant problem which caused difficulties in the simulation was the inability to create a simulation file in which PSPICE could reliably calculate a bias point

prior to the transient analysis. By relaxing the tolerances of the calculations to establish a bias point, the simulation would advance to completion but, the results were suspicious and did not reflect observed results. A solution to this problem was to isolate the components of the circuit into subcircuits and then connect the subcircuits together for simulation. This technique did not result in any functional changes to the actual circuit but, it did provide for a format that allowed PSPICE to calculate a bias point without reducing the tolerance requirements. The new simulation format produced results representative of the original design performance observed in laboratory testing. Based on that experience, it was determined that this format would provide very accurate simulations of the new design. Confidence in the new design's ability to meet the desired performance criteria was increased and the simulations provided insights into design changes that would enhance the performance of the overall design. Figure 8.5 and Figure 8.6 contain PSPICE plots of the simulation results of gain bandwidth product determinations. Based on these results the gain bandwith product of the TSC_C2OA-2 was estimated to be 4 MHz. The input signal was a 0.1 Volt peak sine wave at 300 KHz and 400 KHz respectively.

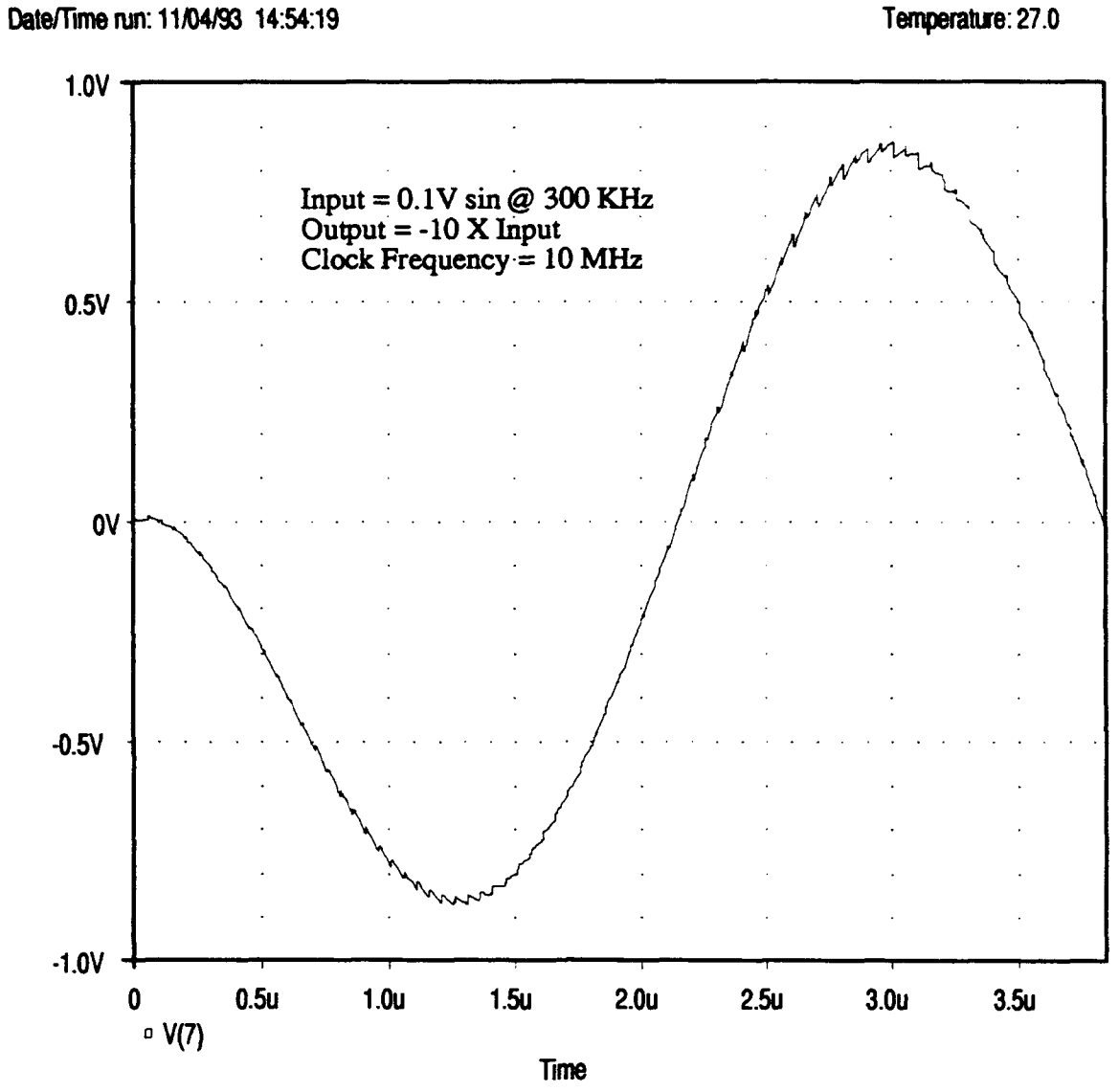


Figure 8.5 Bandwidth Simulations For TSC_C2OA-2 at 300 KHz

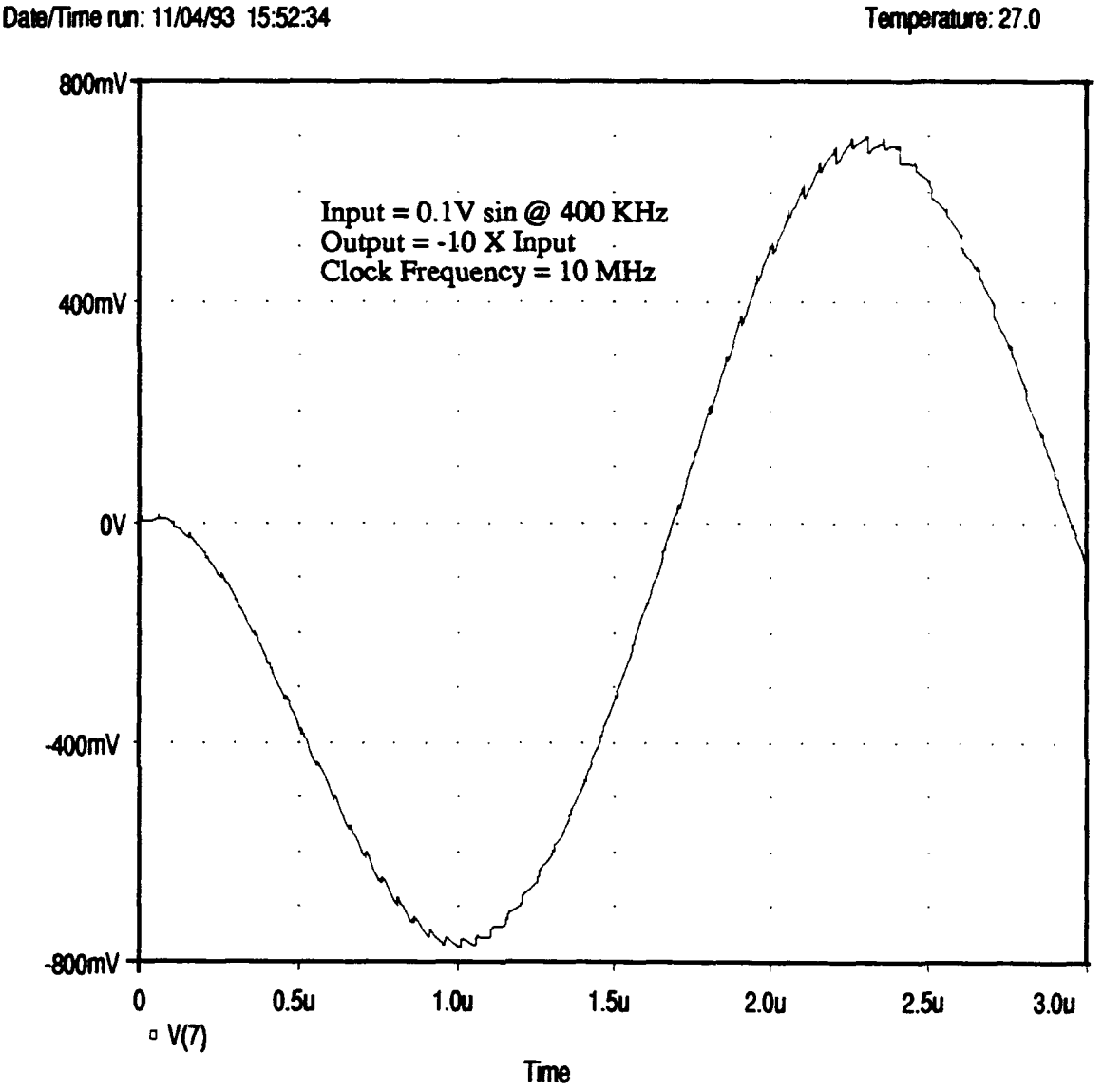


Figure 8.6 Bandwidth Simulations For TSC_C2OA-2 at 400 KHz

IX. CONCLUSIONS AND RECOMMENDATIONS

A. CONCLUSIONS

This thesis represents the first CMOS stray insensitive switched capacitor network to be designed, simulated, fabricated and laboratory tested at the Naval Postgraduate School. VLSI technology and a fully custom process was utilized to provide the maximum design flexibility. Although the test results from the first microchip design did not perform up to expectations, it did provide enough information to demonstrate proof of concept. Information and experience gained from the fabrication and testing of the first design were used to improve the design of the second microchip. Also, the availability of a VLSI process optimized for low noise analog circuits and increased emphasis on design considerations should substantially reduce the noise in the analog signal path.

The scope of this work covers the complete design, simulation, fabrication, testing and resimulation of the first generation stray insensitive switched capacitor CNOAs. The scope also covers the knowledge and experience gained from this design that has proceeded the design, simulation and fabrication of the second generation stray insensitive switched capacitor CNOAs. These designs show great promise for use in filtering applications and as building blocks for neural networks.

B. RECOMMENDATIONS FOR FUTURE RESEARCH

There are several areas that could be pursued as follow on projects. The development of s domain transfer functions and transformation into the z domain would provide for more indepth analysis of the circuits stability. This is also necessary so that sensitivity analysis of the network could be performed. Use of these analysis techniques would be very useful when trying to determine the effect of possible design changes. This would also provide for insight into where design changes should be made to improve the circuit's performance.

Another area that could be pursued is to further improve the CMOS operational amplifier. The open loop gain could be improved by an order of magnitude by using cascode loading on the differential input pair. Also, the output impedance could be reduced by placing several output driver stages in parallel. This would also improve the drive capability of the OA. In addition, the two operational amplifiers in the CNOAs could be optimized for bandwidth and slew rate which would improve the performance of the design.

Improvements could be made in the circuit simulation, especially in the early design evaluations, by purchasing a software package called Switcap. This package is specifically designed for simulating switched capacitor networks. This would reduce the length of time required for simulations and would provide a more flexible tool when attempting to investigate the frequency response of the circuit.

Finally, if the second microchip demonstrates that the noise problems have been solved, then a follow on project could be to optimize the layout area of the design. This

would be important to provide more capability within the relatively small layout area. Also, it is expensive to not utilize the chip area in the most efficient manner possible. The optimization of layout area would allow for more functionality and is always an important goal for VLSI circuit implementations.

APPENDIX A

A. PSPICE Simulation File For Figure 4.7 and Figure 4.8

```
** SPICE file created for circuit cmosamp3
** Technology: scmos
**

* SPICE3C PMOS and NMOS model level 2 nominal paramters,
* derived from corner parameters above.

.MODEL npf PMOS(LEVEL=2 VTO=-0.75 TOX=400E-10 NSUB=6.0E+15
+ XJ=0.05U LD=0.20U U0=255 UCRIT=0.86E5 UEXP=0.29 VMAX=3.0E4
+ NEFF=2.65 DELTA=1.0 RSH=101 CGSO=1.9E-10 CGDO=1.9E-10
+ CJ=250U CJSW=350P MJ=0.535 MJSW=0.34 PB=0.8)

.MODEL nnf NMOS(LEVEL=2 VTO=+0.775 TOX=400E-10 NSUB=8.0E+15
+ XJ=0.15U LD=0.20U U0=650 UCRIT=0.62E5 UEXP=0.125 VMAX=5.1E4
+ NEFF=4.0 DELTA=1.4 RSH=36 CGSO=1.95E-10 CGDO=1.95E-10
+ CJ=195U CJSW=500P MJ=0.76 MJSW=0.30 PB=0.8)

*Power Supplies
VDD 100 0 5
VSS 105 0 -5
VINVERT 111 0 AC 0.0001
VNONINVERT 110 0 0
*VIN 111 0 PULSE(1 -1 4us 2ns 2ns 10us 20us)

*Feedback
*RF 8 2 50K
*RIN 12 2 500
*CLD 102 105 10P
CC 106 102 10P


M0 100 101 102 100 npf L=4.0U W=66.0U
M1 103 103 100 100 npf L=4.0U W=24.0U
M2 102 104 105 105 nnf L=4.0U W=20.0U
M3 100 101 104 105 nnf L=70.0U W=4.0U
```

```
M4 106 105 101 100 npf L=10.0U W=10.0U
M5 104 107 105 105 nnf L=4.0U W=28.0U
M6 100 108 101 100 npf L=4.0U W=24.0U
M7 108 108 100 100 npf L=4.0U W=24.0U
M8 103 103 107 105 nnf L=186.0U W=4.0U
M9 109 107 105 105 nnf L=4.0U W=21.0U
M10 109 110 101 105 nnf L=4.0U W=26.0U
M11 108 111 109 105 nnf L=4.0U W=26.0U
M12 105 107 107 105 nnf L=4.0U W=11.0U
C0 106 102 5103F
** NODE: 111 = VIN-
** NODE: 110 = VIN+
C1 109 105 87F
** NODE: 109 = 6_186_159#
C2 107 105 54F
** NODE: 107 = 6_178_163#
C3 108 105 106F
** NODE: 108 = 6_228_77#
C4 105 105 181F
** NODE: 105 = Vss
C5 104 105 77F
** NODE: 104 = 6_186_89#
C6 100 105 263F
** NODE: 100 = Vdd
C7 102 105 161F
** NODE: 102 = OUT
C8 106 105 2913F
** NODE: 106 = 6_329_161#
C9 103 105 157F
** NODE: 103 = 6_286_77#
C10 101 105 165F
** NODE: 101 = 6_218_159#

*Simulation parameters for frequency response
.AC DEC 20 1 100MEG

*Simulation parameters for transient response
*.TRAN .2us 24us
.PROBE
.END
```

B. PSPICE Simulation File For Figure 6.4 through Figure 6.7

```
** SPICE file created for circuit nvclk2
** Technology: scmos
**

.MODEL npf PMOS(LEVEL=2 VTO=-0.75 TOX=400E-10 NSUB=6.0E+15
+ XJ=0.05U LD=0.20U U0=255 UCRIT=0.86E5 UEXP=0.29 VMAX=3.0E4
+ NEFF=2.65 DELTA=1.0 RSH=101 CGSO=1.9E-10 CGDO=1.9E-10
+ CJ=250U CJSW=350P MJ=0.535 MJSW=0.34 PB=0.8)

.MODEL nnf NMOS(LEVEL=2 VTO=+0.775 TOX=400E-10 NSUB=8.0E+15
+ XJ=0.15U LD=0.20U U0=650 UCRIT=0.62E5 UEXP=0.125 VMAX=5.1E4
+ NEFF=4.0 DELTA=1.4 RSH=36 CGSO=1.95E-10 CGDO=1.95E-10
+ CJ=195U CJSW=500P MJ=0.76 MJSW=0.30 PB=0.8)

*Power Supplies
VDD 102 0 5
VSS 103 0 -5
VIN 110 0 PULSE(5 0 0.1us 2ns 2ns 0.05us 0.1us)

M0 100 101 102 102 npf L=2.0U W=28.0U
M1 103 101 100 103 nnf L=2.0U W=12.0U
M2 101 104 102 102 npf L=2.0U W=28.0U
M3 103 104 101 103 nnf L=2.0U W=12.0U
M4 104 105 102 102 npf L=2.0U W=14.0U
M5 103 105 104 103 nnf L=2.0U W=6.0U
M6 105 106 102 102 npf L=2.0U W=14.0U
M7 103 106 105 103 nnf L=2.0U W=6.0U
M8 102 107 108 102 npf L=2.0U W=7.0U
M9 108 109 106 102 npf L=2.0U W=7.0U
M10 106 107 103 103 nnf L=2.0U W=3.0U
M11 106 109 103 103 nnf L=2.0U W=3.0U
M12 107 110 102 102 npf L=2.0U W=7.0U
M13 103 110 107 103 nnf L=2.0U W=3.0U
M14 109 111 102 102 npf L=2.0U W=28.0U
M15 103 111 109 103 nnf L=2.0U W=12.0U
M16 111 112 102 102 npf L=2.0U W=28.0U
M17 103 112 111 103 nnf L=2.0U W=12.0U
M18 112 113 102 102 npf L=2.0U W=14.0U
M19 103 113 112 103 nnf L=2.0U W=6.0U
M20 113 114 102 102 npf L=2.0U W=14.0U
M21 103 114 113 103 nnf L=2.0U W=6.0U
```

```
M22 102 110 115 102 npf L=2.0U W=7.0U
M23 115 100 114 102 npf L=2.0U W=7.0U
M24 114 110 103 103 nnf L=2.0U W=3.0U
M25 114 100 103 103 nnf L=2.0U W=3.0U
** NODE: 115 = 2_input_nor_1/6_33_14#
C0 114 0 59F
** NODE: 114 = inverter2_0/IN
C1 113 0 68F
** NODE: 113 = inverter2_1/IN
C2 112 0 68F
** NODE: 112 = inverter4_2/IN
C3 103 0 246F
** NODE: 103 = Vss
C4 109 0 119F
** NODE: 109 = P2
C5 111 0 111F
** NODE: 111 = NP2
C6 110 0 25F
** NODE: 110 = CLK
** NODE: 108 = 2_input_nor_0/6_33_14#
C7 107 0 47F
** NODE: 107 = inverter_8/OUT
C8 106 0 59F
** NODE: 106 = inverter2_2/IN
C9 105 0 68F
** NODE: 105 = inverter2_3/IN
C10 104 0 68F
** NODE: 104 = inverter4_0/IN
C11 100 0 118F
** NODE: 100 = P1
C12 102 0 316F
** NODE: 102 = Vdd
C13 101 0 113F
** NODE: 101 = NP1

*Simulation parameters for transient response
.TRAN .01us 1us
.PROBE
.END
```

C. PSPICE Simulation File For Figure 7.5

```
** SPICE file created for circuit cmosamp3
** Technology: scmos
**

* SPICE3C PMOS and NMOS model level 2 nominal paramters,
* derived from corner parameters above.

.MODEL nnf NMOS (LEVEL=2 PHI=0.600000 TOX=4.1300E-08 XJ=0.200000U
TPG=1
+ VTO=0.7108 DELTA=4.8120E+00 LD=2.9230E-07 KP=4.7115E-05
+ UO=563.5 UEXP=1.5690E-01 UCRIT=1.0980E+05 RSH=2.6430E+01
+ GAMMA=0.5617 NSUB=6.6450E+15 NFS=2.060E+11 VMAX=6.4920E+04
+ LAMBDA=3.2380E-02 CGDO=3.6659E-10 CGSO=3.6659E-10
+ CGBO=3.7314E-10 CJ=1.0789E-04 MJ=0.6654 CJSW=4.5280E-10
+ MJSW=0.310750 PB=0.800000)
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -3.9960E-07

.MODEL npf PMOS (LEVEL=2 PHI=0.600000 TOX=4.1300E-08 XJ=0.200000U
TPG=-1
+ VTO=-0.7905 DELTA=2.7300E+00 LD=2.8650E-07 KP=2.1087E-05
+ UO=252.2 UEXP=2.6920E-01 UCRIT=4.6950E+04 RSH=7.3710E+01
+ GAMMA=0.6379 NSUB=8.5700E+15 NFS=2.770E+11 VMAX=9.9990E+05
+ LAMBDA=4.4130E-02 CGDO=3.5932E-10 CGSO=3.5932E-10
+ CGBO=4.3195E-10 CJ=2.5057E-04 MJ=0.5508 CJSW=2.8373E-10
+ MJSW=0.273554 PB=0.800000)
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -4.6260E-07

*Power Supplies
VDD 1 0 5
VSS 3 0 -5
VINVERT 2 0 AC 0.0001
VNONINVERT 4 0 0
*VIN 2 0 PULSE(1 -1 4us 2ns 2ns 10us 20us)

*Feedback
*RF 8 2 50K
*RIN 12 2 500
*RBIAS 8 3 50K
CLD 8 3 10P
```

```
** NODE: 0 = GND
** NODE: 1 = Vdd
** NODE: 2 = Error
M1 5 2 7 3 nnf L=8.0U W=200.0U
M2 6 4 7 3 nnf L=8.0U W=200.0U
M3 5 5 1 1 npf L=10.0U W=60.0U
M4 6 5 1 1 npf L=10.0U W=60.0U
M5 7 10 3 3 nnf L=10.0U W=53.0U
M6 8 6 1 1 npf L=8.0U W=320.0U
M7 8 9 3 3 nnf L=7.0U W=100.0U
M8 6 3 21 1 npf L=10.0U W=10.0U
M9 1 6 9 3 nnf L=176.0U W=10.0U
M10 9 10 3 3 nnf L=10.0U W=71.0U
M11 11 11 1 1 npf L=10.0U W=66.0U
M12 11 11 10 3 nnf L=484.0U W=10.0U
M13 10 10 3 3 nnf W=27.0U L=10.0U

*Compensation capacitor
CC 21 8 10P


*Simulation parameters for frequency response
.AC DEC 20 1 100MEG
*.TRAN .2us 24us

.PROBE
.END
```

D. PSPICE Simulation File For Figure 7.7

```
** SPICE file created to test TSC_C2OA-2 with switch capacitors
**

.SUBCKT OPAMP1 110 111 100
*INVERTING INPUT 111
*NONINVERTING INPUT 110
*OUTPUT 100

*N29T  SPICE LEVEL 2 PARAMETERS

.MODEL npf PMOS(LEVEL=2 VTO=-0.75 TOX=400E-10 NSUB=6.0E+15
+ XJ=0.05U LD=0.20U U0=255 UCRIT=0.86E5 UEXP=0.29 VMAX=3.0E4
```

```
+ NEFF=2.65 DELTA=1.0 RSH=101 CGSO=1.9E-10 CGDO=1.9E-10
+ CJ=250U CJSW=350P MJ=0.535 MJSW=0.34 PB=0.8)

.MODEL nnf NMOS(LEVEL=2 VTO=+0.775 TOX=400E-10 NSUB=8.0E+15
+ XJ=0.15U LD=0.20U U0=650 UCRIT=0.62E5 UEXP=0.125 VMAX=5.1E4
+ NEFF=4.0 DELTA=1.4 RSH=36 CGSO=1.95E-10 CGDO=1.95E-10
+ CJ=195U CJSW=500P MJ=0.76 MJSW=0.30 PB=0.8)


*.MODEL nnf NMOS (LEVEL=2 PHI=0.600000 TOX=4.1300E-08 XJ=0.200000U
TPG=1
*+ VTO=0.7108 DELTA=4.8120E+00 LD=2.9230E-07 KP=4.7115E-05
*+ UO=563.5 UEXP=1.5690E-01 UCRIT=1.0980E+05 RSH=2.6430E+01
*+ GAMMA=0.5617 NSUB=6.6450E+15 NFS=2.060E+11 VMAX=6.4920E+04
*+ LAMBDA=3.2380E-02 CGDO=3.6659E-10 CGSO=3.6659E-10
*+ CGBO=3.7314E-10 CJ=1.0789E-04 MJ=0.6654 CJSW=4.5280E-10
*+ MJSW=0.310750 PB=0.800000)
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -3.9960E-07

*.MODEL npf PMOS (LEVEL=2 PHI=0.600000 TOX=4.1300E-08 XJ=0.200000U
TPG=-1
*+ VTO=-0.7905 DELTA=2.7300E+00 LD=2.8650E-07 KP=2.1087E-05
*+ UO=252.2 UEXP=2.6920E-01 UCRIT=4.6950E+04 RSH=7.3710E+01
*+ GAMMA=0.6379 NSUB=8.5700E+15 NFS=2.770E+11 VMAX=9.9990E+05
*+ LAMBDA=4.4130E-02 CGDO=3.5932E-10 CGSO=3.5932E-10
*+ CGBO=4.3195E-10 CJ=2.5057E-04 MJ=0.5508 CJSW=2.8373E-10
*+ MJSW=0.273554 PB=0.800000)
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -4.6260E-07


*Power Supplies
VDD 102 0 5
VSS 105 0 -5

M0 102 101 100 102 npf L=4.0U W=66.0U
M1 103 103 102 102 npf L=4.0U W=24.0U
M2 100 104 105 105 nnf L=4.0U W=20.0U
M3 102 101 104 105 nnf L=70.0U W=4.0U
M4 106 105 101 102 npf L=10.0U W=10.0U
M5 104 107 105 105 nnf L=4.0U W=28.0U
M6 102 108 101 102 npf L=4.0U W=24.0U
```

```
M7 108 108 102 102 npf L=4.0U W=24.0U
M8 103 103 107 105 nnf L=186.0U W=4.0U
M9 109 107 105 105 nnf L=4.0U W=21.0U
M10 109 110 101 105 nnf L=4.0U W=26.0U
M11 108 111 109 105 nnf L=4.0U W=26.0U
M12 105 107 107 105 nnf L=4.0U W=11.0U

C0 106 100 7029F
C1 109 105 87F
C2 107 105 54F
C3 108 105 106F
C5 104 105 77F
C6 100 105 306F
C7 102 105 165F
C8 106 105 2874F
C9 103 105 157F
C10 101 105 165F

.ENDS OPAMP1

.SUBCKT CLOCK  312 300 311 301 313
*MASTER CLOCK 312     P1 300     P2 311     NP1 301     NP2 313

.MODEL npf PMOS(LEVEL=2 VTO=-0.75 TOX=400E-10 NSUB=6.0E+15
+ XJ=0.05U LD=0.20U U0=255 UCRIT=0.86E5 UEXP=0.29 VMAX=3.0E4
+ NEFF=2.65 DELTA=1.0 RSH=101 CGSO=1.9E-10 CGDO=1.9E-10
+ CJ=250U CJSW=350P MJ=0.535 MJSW=0.34 PB=0.8)

.MODEL nnf NMOS(LEVEL=2 VTO=+0.775 TOX=400E-10 NSUB=8.0E+15
+ XJ=0.15U LD=0.20U U0=650 UCRIT=0.62E5 UEXP=0.125 VMAX=5.1E4
+ NEFF=4.0 DELTA=1.4 RSH=36 CGSO=1.95E-10 CGDO=1.95E-10
+ CJ=195U CJSW=500P MJ=0.76 MJSW=0.30 PB=0.8)


*Power Supplies
VDD 102 0 5
VSS 105 0 -5

M0 300 301 102 102 npf L=2.0U W=28.0U
M1 105 301 300 105 nnf L=2.0U W=12.0U
M2 301 304 102 102 npf L=2.0U W=28.0U
M3 105 304 301 105 nnf L=2.0U W=12.0U
M4 304 305 102 102 npf L=2.0U W=14.0U
```

```
M5 105 305 304 105 nnf L=2.0U W=6.0U
M6 305 306 102 102 npf L=2.0U W=14.0U
M7 105 306 305 105 nnf L=2.0U W=6.0U
M8 306 307 102 102 npf L=2.0U W=7.0U
M9 105 307 306 105 nnf L=2.0U W=3.0U
M10 307 308 102 102 npf L=2.0U W=7.0U
M11 105 308 307 105 nnf L=2.0U W=3.0U
M12 102 309 310 102 npf L=2.0U W=7.0U
M13 310 311 308 102 npf L=2.0U W=7.0U
M14 308 309 105 105 nnf L=2.0U W=3.0U
M15 308 311 105 105 nnf L=2.0U W=3.0U
M16 309 312 102 102 npf L=2.0U W=7.0U
M17 105 312 309 105 nnf L=2.0U W=3.0U
M18 311 313 102 102 npf L=2.0U W=28.0U
M19 105 313 311 105 nnf L=2.0U W=12.0U
M20 313 314 102 102 npf L=2.0U W=28.0U
M21 105 314 313 105 nnf L=2.0U W=12.0U
M22 314 315 102 102 npf L=2.0U W=14.0U
M23 105 315 314 105 nnf L=2.0U W=6.0U
M24 315 316 102 102 npf L=2.0U W=14.0U
M25 105 316 315 105 nnf L=2.0U W=6.0U
M26 316 317 102 102 npf L=2.0U W=7.0U
M27 105 317 316 105 nnf L=2.0U W=3.0U
M28 317 318 102 102 npf L=2.0U W=7.0U
M29 105 318 317 105 nnf L=2.0U W=3.0U
M30 102 312 319 102 npf L=2.0U W=7.0U
M31 319 300 318 102 npf L=2.0U W=7.0U
M32 318 312 105 105 nnf L=2.0U W=3.0U
M33 318 300 105 105 nnf L=2.0U W=3.0U

C0 318 105 60F
C1 317 105 46F
C2 316 105 46F
C3 315 105 68F
C4 314 105 68F
C5 105 105 326F
C6 311 105 125F
C7 313 105 118F
C8 312 105 28F
C9 309 105 50F
C10 308 105 60F
C11 307 105 46F
C12 306 105 46F
```

```
C13 305 105 68F
C14 304 105 68F
C15 300 105 120F
C16 102 105 390F
C17 301 105 121F

.ENDS CLOCK

.SUBCKT SWITCH  104  106  100  103  108  101  107
*IN1 104     IN2 106     OUT 100     P1 103      P2 108
*NP1 101     NP2 107

.MODEL npf PMOS(LEVEL=2 VTO=-0.75 TOX=400E-10 NSUB=6.0E+15
+ XJ=0.05U LD=0.20U U0=255 UCRIT=0.86E5 UEXP=0.29 VMAX=3.0E4
+ NEFF=2.65 DELTA=1.0 RSH=101 CGSO=1.9E-10 CGDO=1.9E-10
+ CJ=250U CJSW=350P MJ=0.535 MJSW=0.34 PB=0.8)

.MODEL nnf NMOS(LEVEL=2 VTO=+0.775 TOX=400E-10 NSUB=8.0E+15
+ XJ=0.15U LD=0.20U U0=650 UCRIT=0.62E5 UEXP=0.125 VMAX=5.1E4
+ NEFF=4.0 DELTA=1.4 RSH=36 CGSO=1.95E-10 CGDO=1.95E-10
+ CJ=195U CJSW=500P MJ=0.76 MJSW=0.30 PB=0.8)

VDD 102 0 5
VSS 105 0 -5

M0 100 101 104 102 npf L=2.0U W=60.0U
M1 104 101 100 102 npf L=2.0U W=60.0U
M2 100 103 104 105 nnf L=2.0U W=45.0U
M3 104 103 100 105 nnf L=2.0U W=45.0U
C0 100 105 169F
C1 104 105 383F
M4 100 107 106 102 npf L=2.0U W=60.0U
M5 106 107 100 102 npf L=2.0U W=60.0U
M6 100 108 106 105 nnf L=2.0U W=45.0U
M7 106 108 100 105 nnf L=2.0U W=45.0U
C2 100 105 169F
C3 106 105 383F

.ENDS SWITCH

*Power Supplies
VIN 3 0 SIN(0 0.1 10KHz)
VCLK 8 0 PULSE(5 -5 0.0us 2ns 2ns 0.05us 0.1us)
```

```
X1   0  4  5              OPAMP1
X2   5  6  7              OPAMP1
X3   8  9 10 11 12          CLOCK
X4   0  7 15  9 10 11 12   SWITCH
X5   6  0 18  9 10 11 12   SWITCH
X6   0  6 21  9 10 11 12   SWITCH
X7   0  0 24  9 10 11 12   SWITCH

C   24 21    0.7P
CA  18 15     4.3P
CF1  7  6     50P
CF2  4  5     50P
CLD  7  0     2200P

*Feedback
RF   7 4 100K
RIN 3 4 10K

.TRAN .01us 100us
.PROBE
.END
```

E. PSPICE Simulation File For Figure 8.5 and Figure 8.6

```
**SUBCIRCUIT DEFINITION


.SUBCKT OPAMP1 110 111 101
*INVERTING INPUT 111
*NONINVERTING INPUT 110
*OUTPUT 101

*N29T  SPICE LEVEL 2 PARAMETERS

.MODEL nnf NMOS (LEVEL=2 PHI=0.600000 TOX=4.1600E-08 XJ=0.250000U
TPG=1
+ VTO=0.8679 DELTA=4.0030E+00 LD=1.9290E-07 KP=4.9888E-05
+ UO=601.0 UEXP=1.6020E-01 UCRIT=8.0970E+04 RSH=2.3630E+01
+ GAMMA=0.5303 NSUB=5.8370E+15 NFS=4.5450E+12 VMAX=6.1580E+04
+ LAMBDA=2.9870E-02 CGDO=2.4018E-10 CGSO=2.4018E-10
+ CGBO=4.0974E-10 CJ=1.0068E-04 MJ=0.8562 CJSW=4.6535E-10
```

```
+ MJSW=0.343293 PB=0.800000)
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -3.9960E-07

.MODEL npf PMOS (LEVEL=2 PHI=0.600000 TOX=4.1600E-08 XJ=0.250000U
TPG=-1
+ VTO=-0.9403 DELTA=4.6650E+00 LD=3.4100E-07 KP=1.8378E-05
+ UO=221.4 UEXP=2.5580E-01 UCRIT=5.1320E+04 RSH=6.1590E+01
+ GAMMA=0.7010 NSUB=1.0200E+16 NFS=4.5550E+12 VMAX=9.9990E+05
+ LAMBDA=4.3880E-02 CGDO=4.2459E-10 CGSO=4.2459E-10
+ CGBO=4.1990E-10 CJ=3.1845E-04 MJ=0.5734 CJSW=3.5031E-10
+ MJSW=0.337596 PB=0.800000)
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -4.6260E-07

*Power Supplies
VDD 102 0 5
VSS 105 0 -5


M1 102 103 101 102 npf L=10.0U W=164.0U
M2 104 104 102 102 npf L=10.0U W=66.0U
M3 103 105 100 102 npf L=10.0U W=10.0U
M4 101 106 105 105 nnf L=9.0U W=50.0U
M5 106 107 105 105 nnf L=10.0U W=71.0U
M6 102 103 106 105 nnf L=176.0U W=10.0U
M7 108 107 105 105 nnf L=10.0U W=53.0U
M8 102 109 103 102 npf L=10.0U W=60.0U
M9 109 109 102 102 npf L=10.0U W=60.0U
M10 108 110 103 105 nnf L=10.0U W=66.0U
M11 109 111 108 105 nnf L=10.0U W=66.0U
M12 104 104 107 105 nnf L=460.0U W=10.0U
M13 105 107 107 105 nnf L=10.0U W=27.0U

C0 105 105 375F
C1 109 105 259F
C2 108 105 235F
C3 107 105 118F
C4 106 105 49F
C5 102 105 657F
C6 101 105 1097F
C7 100 105 119F
C8 104 105 436F
```

```
C9 103 105 381F

CC 100 101 5P
.ENDS OPAMP1

.SUBCKT SWITCH 103 107 100 106 108 104 101
*IN1 103    IN2 107    OUT 100    P1 106    P2 108
*NP1 104    NP2 101

.MODEL nnf NMOS (LEVEL=2 PHI=0.600000 TOX=4.1600E-08 XJ=0.250000U
TPG=1
+ VTO=0.8679 DELTA=4.0030E+00 LD=1.9290E-07 KP=4.9888E-05
+ UO=601.0 UEXP=1.6020E-01 UCRIT=8.0970E+04 RSH=2.3630E+01
+ GAMMA=0.5303 NSUB=5.8370E+15 NFS=4.5450E+12 VMAX=6.1580E+04
+ LAMBDA=2.9870E-02 CGDO=2.4018E-10 CGSO=2.4018E-10
+ CGBO=4.0974E-10 CJ=1.0068E-04 MJ=0.8562 CJSW=4.6535E-10
+ MJSW=0.343293 PB=0.800000)
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -3.9960E-07

.MODEL npf PMOS (LEVEL=2 PHI=0.600000 TOX=4.1600E-08 XJ=0.250000U
TPG=-1
+ VTO=-0.9403 DELTA=4.6650E+00 LD=3.4100E-07 KP=1.8378E-05
+ UO=221.4 UEXP=2.5580E-01 UCRIT=5.1320E+04 RSH=6.1590E+01
+ GAMMA=0.7010 NSUB=1.0200E+16 NFS=4.5550E+12 VMAX=9.9990E+05
+ LAMBDA=4.3880E-02 CGDO=4.2459E-10 CGSO=4.2459E-10
+ CGBO=4.1990E-10 CJ=3.1845E-04 MJ=0.5734 CJSW=3.5031E-10
+ MJSW=0.337596 PB=0.800000)
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -4.6260E-07

*Power Supplies
VDD 102 0 5
VSS 105 0 -5


M0 100 101 107 102 npf L=2.0U W=7.0U
M1 103 104 100 102 npf L=2.0U W=7.0U
M2 100 108 107 105 nnf L=2.0U W=4.0U
M3 103 106 100 105 nnf L=2.0U W=4.0U

C0 103 105 29F
C1 100 105 29F
```

```
C2 108 105 29F

.ENDS SWITCH

.SUBCKT CLOCK  312 300 311 301 313
*MASTER CLOCK 312     P1 300     P2 311     NP1 301     NP2 313

.MODEL nnf NMOS (LEVEL=2 PHI=0.600000 TOX=4.1600E-08 XJ=0.250000U
TPG=1
+ VTO=0.8679 DELTA=4.0030E+00 LD=1.9290E-07 KP=4.9888E-05
+ UO=601.0 UEXP=1.6020E-01 UCRIT=8.0970E+04 RSH=2.3630E+01
+ GAMMA=0.5303 NSUB=5.8370E+15 NFS=4.5450E+12 VMAX=6.1580E+04
+ LAMBDA=2.9870E-02 CGDO=2.4018E-10 CGSO=2.4018E-10
+ CGBO=4.0974E-10 CJ=1.0068E-04 MJ=0.8562 CJSW=4.6535E-10
+ MJSW=0.343293 PB=0.800000)
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -3.9960E-07

.MODEL npf PMOS (LEVEL=2 PHI=0.600000 TOX=4.1600E-08 XJ=0.250000U
TPG=-1
+ VTO=-0.9403 DELTA=4.6650E+00 LD=3.4100E-07 KP=1.8378E-05
+ UO=221.4 UEXP=2.5580E-01 UCRIT=5.1320E+04 RSH=6.1590E+01
+ GAMMA=0.7010 NSUB=1.0200E+16 NFS=4.5550E+12 VMAX=9.9990E+05
+ LAMBDA=4.3880E-02 CGDO=4.2459E-10 CGSO=4.2459E-10
+ CGBO=4.1990E-10 CJ=3.1845E-04 MJ=0.5734 CJSW=3.5031E-10
+ MJSW=0.337596 PB=0.800000)
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -4.6260E-07


*Power Supplies
VDD 102 0 5
VSS 105 0 -5

M0 300 301 102 102 npf L=2.0U W=28.0U
M1 105 301 300 105 nnf L=2.0U W=12.0U
M2 301 304 102 102 npf L=2.0U W=28.0U
M3 105 304 301 105 nnf L=2.0U W=12.0U
M4 304 305 102 102 npf L=2.0U W=14.0U
M5 105 305 304 105 nnf L=2.0U W=6.0U
M6 305 306 102 102 npf L=2.0U W=14.0U
M7 105 306 305 105 nnf L=2.0U W=6.0U
M8 306 307 102 102 npf L=2.0U W=7.0U
```

```
M9 105 307 306 105 nnf L=2.0U W=3.0U
M10 307 308 102 102 npf L=2.0U W=7.0U
M11 105 308 307 105 nnf L=2.0U W=3.0U
M12 102 309 310 102 npf L=2.0U W=7.0U
M13 310 311 308 102 npf L=2.0U W=7.0U
M14 308 309 105 105 nnf L=2.0U W=3.0U
M15 308 311 105 105 nnf L=2.0U W=3.0U
M16 309 312 102 102 npf L=2.0U W=7.0U
M17 105 312 309 105 nnf L=2.0U W=3.0U
M18 311 313 102 102 npf L=2.0U W=28.0U
M19 105 313 311 105 nnf L=2.0U W=12.0U
M20 313 314 102 102 npf L=2.0U W=28.0U
M21 105 314 313 105 nnf L=2.0U W=12.0U
M22 314 315 102 102 npf L=2.0U W=14.0U
M23 105 315 314 105 nnf L=2.0U W=6.0U
M24 315 316 102 102 npf L=2.0U W=14.0U
M25 105 316 315 105 nnf L=2.0U W=6.0U
M26 316 317 102 102 npf L=2.0U W=7.0U
M27 105 317 316 105 nnf L=2.0U W=3.0U
M28 317 318 102 102 npf L=2.0U W=7.0U
M29 105 318 317 105 nnf L=2.0U W=3.0U
M30 102 312 319 102 npf L=2.0U W=7.0U
M31 319 300 318 102 npf L=2.0U W=7.0U
M32 318 312 105 105 nnf L=2.0U W=3.0U
M33 318 300 105 105 nnf L=2.0U W=3.0U

C0 318 105 60F
C1 317 105 46F
C2 316 105 46F
C3 315 105 68F
C4 314 105 68F
C5 105 105 326F
C6 311 105 125F
C7 313 105 118F
C8 312 105 28F
C9 309 105 50F
C10 308 105 60F
C11 307 105 46F
C12 306 105 46F
C13 305 105 68F
C14 304 105 68F
C15 300 105 120F
C16 102 105 390F
```

```
C17 301 105 121F

.ENDS CLOCK

*Power Supplies
VIN 3 0 SIN(0 0.1 400KHz)
VCLK 8 0 PULSE(5 -5 0.0us 2ns 2ns 0.05us 0.1us)

X1   0  4  5              OPAMP1
X2   5  6  7              OPAMP1
X3   8  9 10 11 12          CLOCK
X4   0  7 15  9 10 11 12   SWITCH
X5   6  0 18  9 10 11 12   SWITCH
X6   0  6 21  9 10 11 12   SWITCH
X7   0  0 24  9 10 11 12   SWITCH

C   24 21    .1P
CA  18 15    .1P
CF1  7  6    10P
CLD  7  0    10P

*Feedback
RF  7 4 100K
RIN 3 4 10K

.TRAN .00002us 2.3us
.PROBE v(3),v(7)
.END
```

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